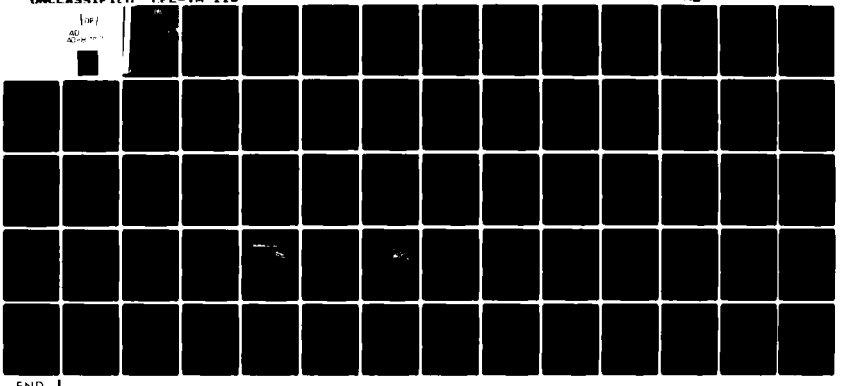
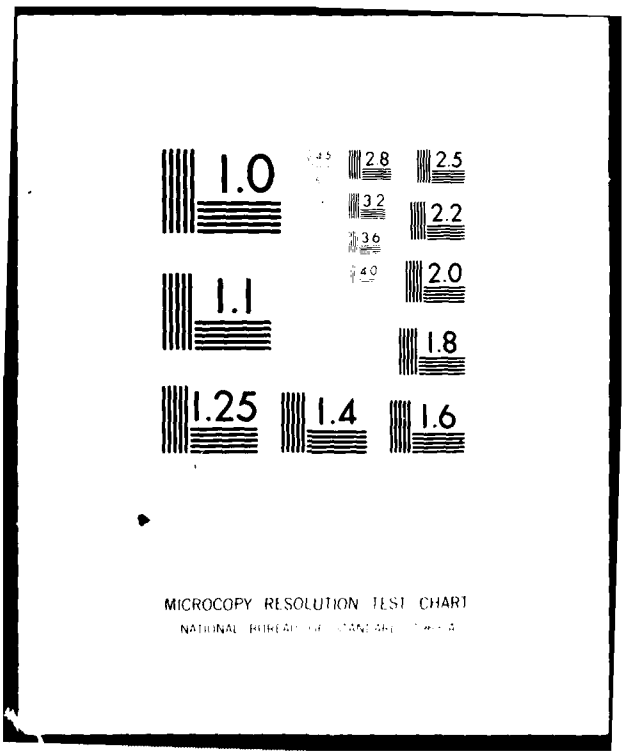
AD-A088 757 MICHIGAN UNIV ANN ARBOR COOLEY ELECTRONICS LAB F/G 14/2
THE 1979 TOWED SOURCE EXPERIMENT SIGNAL GENERATOR.(U)
DEC 79 K METZGER, L W VON WALD N00014-75-C-0127
UNCLASSIFIED CEL-TM-116 NL



END
DATE FILMED
10-80
DTIC


1.0
2.8
2.5
3.2
2.2
3.6
4.0
2.0
1.1
1.8
1.25
1.4
1.6
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS

Report 013376-9-M

THE 1979 TOWED SOURCE EXPERIMENT SIGNAL GENERATOR

K. Metzger, Jr.
L. W. Von Wald

COOLEY ELECTRONICS LABORATORY
Department of Electrical and Computer Engineering
The University of [redacted]
Ann Arbor, Michigan 48109

December 1979

Technical Memorandum No. 116

Approved for public release; distribution unlimited.

Prepared for
OFFICE OF NAVAL RESEARCH
Department of the Navy
Arlington, Virginia 22217

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: 013376-9-M	2. GOVT ACCESSION NO.: AD-A088 757
3. RECIPIENT'S CATALOG NUMBER:	
4. TITLE (and Subtitle): THE 1979 TOWED SOURCE EXPERIMENT SIGNAL GENERATOR.	5. TYPE OF REPORT & PERIOD COVERED: Technical memorandum
	6. PERFORMING ORG. REPORT NUMBER: TM116
7. AUTHOR(s): K. Metzger, Jr. L. W. Von Wald	8. CONTRACT OR GRANT NUMBER(s): N00014-75-C-0175
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Cooley Electronics Laboratory University of Michigan Ann Arbor, Michigan 48109	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 11 Dec 79
11. CONTROLLING OFFICE NAME AND ADDRESS: Office Of Naval Research Department of the Navy Arlington, Virginia 22217	12. REPORT DATE: December 1979 13. NUMBER OF PAGES: 68
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): CEL-TM-116, 013376-9-M	15. SECURITY CLASS. (of this report): 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

SGEN79
Signal generator
Towed source experiment
PANOIC
WHAMMO

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

SGEN79 is the signal generator designed for use in the towed source experiment conducted during June of 1979. The output of this generator can be made up of the sum of as many as six switch selectable waveforms. The amplitude of each waveform can be individually adjusted. The unit provides a quiet period of 20 minutes once every four hours. Clock timing can be derived from an internal oven-controlled crystal or from an external 1 or 5 MHz reference.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE S/N 0102-014-6601

097400 slt

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20.

Self-metering capabilities are provided.

TABLE OF CONTENTS

ACRONYMS

The following acronyms are used in this report:

PANOIC	A towed source experiment in the Pacific conducted in the summer of 1977. The 7 digit sequence used in the 1979 towed source experiment was the same as that used in PANOIC. The digit duration was reduced to 64 carrier cycles per digit.
WHAMMO	Refers to an augmented linear maximal sequence based transmission that is used in propagation studies performed by the Institute for Acoustic Research.

1. Introduction

SGEN79 is the signal generator designed for use in the towed source experiment conducted during June of 1979. The output of this generator can be made up of the sum of as many as six switch selectable waveforms. The amplitude of each waveform can be individually adjusted. The unit provides a quiet period of 20 minutes once every four hours. Clock timing can be derived from an internal oven-controlled crystal or from an external 1 or 5 MHz reference. Self-metering capabilities are provided.

As configured for the June experiment, the following waveforms are provided:

Channel 1..A 7 digit linear maximal sequence is used to phase modulate a sinusoidal carrier using CM (+-45 degrees) modulation. The duration of each digit corresponds to 64 cycles of carrier. The sequence chosen was the same one used in the PANOIC-77 experiment. This seven digit sequence is 1001011.

Channel 2..A 512-digit augmented linear maximal sequence is used to modulate a sinusoidal carrier using CM (+-45 degrees) modulation. The sequence used to modulate the carrier is the one used by the Institute for Acoustic Research in their WHAMMO transmission. The sequence law setting on the BCSG-76 for this sequence is 01257.

Channel 3..A 255-digit linear maximal sequence is used to modulate a sinusoidal carrier using biphase (+-180 degrees) modulation. The duration of each digit corresponds to 250 cycles of carrier. The sequence law setting on the BCSG-76 for the sequence used is 00455.

Channel 4..A CW sinusoid.

Channel 5..A CW sinusoid.

Channel 6..A CW sinusoid. The frequency is determined by the front panel selector switch setting. Provision is made for two frequencies. The clock divide factors for these two frequencies must be preprogrammed into a ROM contained on the associated waveform generator board.

The carrier frequencies of the individual channels can be set to values in the range of 31,250 Hz to 3.125 Hz. The frequencies correspond to 1 MHz divided by 32 times an integer in the range of 1 thru 9999.

2. Front Panel Description

The signal generator front panel is shown in Figure 2.1. This section describes the function of the indicators and controls on this panel.

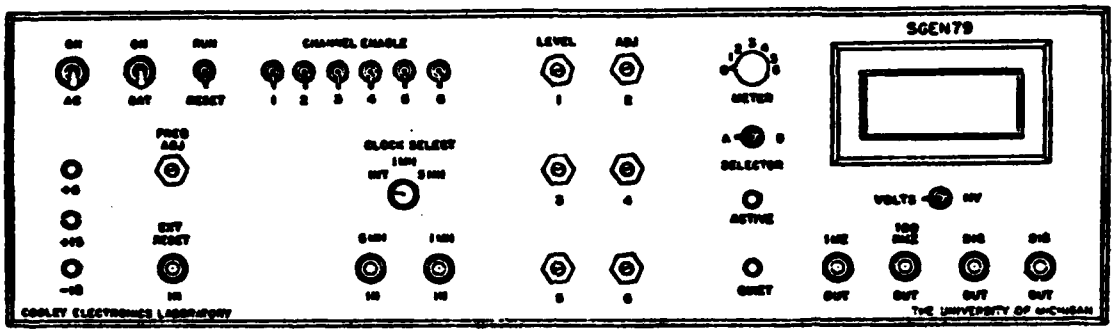


Figure 2.1. SGEN79 Front Panel

AC/ON Toggle Switch

This switch is used to turn on and off the line power to the generator. The line power is on when the switch is in the up position.

BAT/ON Toggle Switch

This switch is used to connect the backup battery supply to the uninterruptible power supply. When this switch is in the up position, the battery is connected and the generator is powered. Normally this switch should only be in the up position when the AC/ON switch is on. The anticipated battery capacity of the SGEN79 battery supply is from one to two hours.

+5 LED

This indicator indicates when the +5 supply is operating. If it is off, it is very likely that the +5 volt supply is not operational. It is not intended to be able to indicate a low voltage situation.

+15 LED

This indicator indicates when the +15 supply is operating. If it is off, it is very likely that the +15 volt supply is not operational. It is not intended to be able to indicate a low voltage situation.

-15 LED

This indicator indicates when the -15 supply is operating. If it is off, it is very likely that the -15 volt supply is not operational. It is not intended to be able to indicate a low voltage situation.

RUN/RESET Toggle Switch

When this toggle switch is in the down (RESET) position, the generator is held in its reset state. All internal timing is suspended and the outputs of any enabled D/A converters are at their maximum values. The off period timer is also reset.

While the generator is in the reset state, the signal output is held at the peak negative excursion value as determined by the level pot settings.

Placing this switch into the up (RUN) position allows normal operation to start. The off period timer starts operation the moment the switch is placed into the RUN position. The first off period will be 3 hours and 40 minutes from this time. The duration of the off period will be 20 minutes. Off periods repeat every four hours (exactly).

EXT RESET IN BNC Connector

This connector makes provision for use of an external signal to reset the generator. To use this input first insure that the RUN/RESET toggle switch is in the RUN position. This input requires a standard TTL compatible drive. A pull-up resistor is provided. Grounding the input causes the unit to enter the reset state. This state is maintained until the ground condition is released. The external BNC signal may then be removed without affecting the unit.

FREQ ADJ Potentiometer

This 10-turn pot is used when setting up the operating frequency of the internal oscillator. The adjustment range is approximately +-1 part in 10^7. The use of this pot is described in the section entitled "Setting the Internal Oscillator."

CLOCK SELECT Rotary Switch

The time base used in this generator can come from three possible sources. These include an internal oven stabilized oscillator, an external 5 MHz source or an external 1 MHz source. It is anticipated that the internal oscillator will normally be used.

5 MHz IN BNC Connector

An external 5 MHz timing signal can be applied here. This signal must be TTL compatible.

1 MHz IN BNC Connector

An external 1 MHz timing signal can be applied here. This signal must be TTL compatible.

CHANNEL ENABLE Toggle Switches 1-6

Each toggle switch turns on or off the D/A converter associated with the indicated channel. A switch in the down position turns off the converter. A switch in the up position turns on the associated converter. These switches do not affect the timing associated with the waveform generation.

The switches for channels 1 and 2 are wired so that when both are in the up position an alarm will sound. This was done because the PANOIC and WHAMMO signals are not to be run at the same time due to transducer power limitations and experiment procedures at the receiving sites. At the sites, only one of these signals could be processed at a given time.

LEVEL Potentiometers 1-6

These six pots are used to adjust the levels of the associated signals. Rotating clockwise increases the signal level. The maximum output contribution from a single channel is 0.701 volts rms.

METER Rotary Switch

This switch is used to select the signal to be applied to the metering circuitry. Positions 1-6 correspond to channels 1 thru 6. Position 0 corresponds to the summed output signal. Channels can only be metered if they are enabled.

VOLTS/MV Toggle Switch

This switch sets the meter sensitivity. The meter display contains three digits. With this switch in the VOLTS position, the display is in volts with the decimal point following the left most digit. With this switch in the MV position, the display is in millivolts with the decimal point following the right most digit.

METER Display

This is a three digit meter. The circuit driving it consists of a full-wave rectifier followed by a two-pole low pass filter. It is calibrated to convert average ac sinusiod levels into rms values. It is not a true rms

meter. Although the display has three digits, it is not fully accurate to that degree.

SELECTOR A/B Toggle Switch

This switch is used to select between two possible operating frequencies for channel 6. The divide factors for the two frequencies are contained in a ROM located on the channel 6 waveform generator board. The channel 6 frequencies can be changed by inserting new ROMs which have been programmed with the desired divide factors. The waveform generator board for channel 6 was modified in order to be controlled by this switch.

ACTIVE LED

This LED is lit when the generator is actively producing an output waveform as determined by the settings of the channel enable toggle switches. It is off when the generator is in a 20-minute quiet period or when the generator is in the reset state.

QUIET LED

This LED is lit when the generator is in the 20-minute quiet period. It is off when the generator is in its active period or when the generator is in the reset state.

1 MHz OUT BNC Connector

A 1 MHz TTL compatible square wave is available here. This waveform is provided for use in adjusting the internal oscillator.

100KHz OUT BNC Connector

A 100 KHz TTL compatible square wave is available here. This waveform is provided for use in adjusting the internal oscillator.

SIG OUT BNC Connectors

These two BNC connectors are wired in parallel. The signal produced by the generator is available on these two connectors. The generator is capable of driving into 600 ohms.

3. Operating Procedure

1. Plug the unit in and turn on the AC power.

2. If the unit contains a battery backup supply, turn on the BATTERY switch. This places the backup batteries into the circuit.

3. Set the CLOCK SELECT switch to choose the desired clock source. This will normally be the INT position. The internal oscillator requires approximately 20 to 30 minutes to warm up and stabilize to a part in 10^8. It is assumed that the internal clock has been previously trimmed.

4. Place the RUN/RESET switch into the RESET position. This completely resets the internal timing circuits and holds the unit in the off state.

5. Place the 6 CHANNEL ENABLE switches in the down position. This turns off the outputs of the 6 internal waveform generators.

6. Place the SELECTOR switch into the A or B position as required.

7. At a convenient time (most likely at the start of an hour divisible by 4, e.g., 0400 or 1200) place the RUN/RESET switch in the RUN position. This enables the internal clocking and allows the output waveforms to be generated. The first off period will be 3 hours and 40 minutes from the time at which the switch is moved from the RESET to the RUN position. Off periods are spaced exactly four hours apart.

8. Set up the signal levels as required by the experiment plan.

   The level setup can be performed using the source transducer monitor (the preferred way) or using the internal metering of the generator.

   Turn on the channel 1 output by placing the channel 1 ENABLE toggle switch in the up position. Adjust the channel 1 level 10-turn pot to obtain the desired level as monitored at the transducer output or as read on the generator meter. Return the channel 1 toggle switch to the down position. The meter channel selector switch should be in the 0 position when making this adjustment. Note that while the meter reads to three significant figures, the metering circuit was built using 1 % parts.

   Repeat the above procedure for channels 2 thru 6. This completes the setup.

9. Turn on the channels required for the current segment of the experiment. This is done by placing the CHANNEL ENABLE toggle switches of the desired channels into the up position.

   If an attempt is made to enable both channels 1 and 2 at the same time, an alarm will sound. The procedure to follow when switching between the PANOIC signal (channel 1) and the WHAMMO signal (channel 2) is to first place both the channel 1 and 2 toggle switches in the down position and then place the enable switch of the desired waveform into the up position.

4. Adjustment

The trim adjustments provided in the generator consist of the waveform generator boards' gain and dc offsets and the oven stabilized oscillator's frequency.

4.1 Setting up the Waveformer Boards

Each waveformer board has two adjustment potentiometers. One of these is used to trim the output D/A converter gain, and the other is used to trim the D/A converter offset voltage. A test point is provided at the front of each board which can be used to monitor the D/A converter output. A top view of the waveformer board showing the locations of the trim pots and the test point is given in Fig. 4.1.

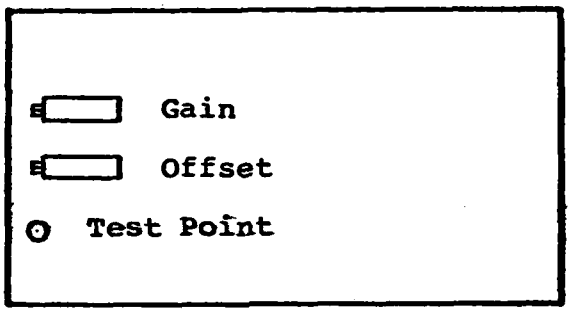


Figure 4.1. Adjustment and test point location

Connect a digital voltmeter between the test point on the board being adjusted and the ground of the +-15 volt supply. Place the RUN/RESET switch on the generator front panel into the RESET position and place the channel select switch for the board being adjusted in the down position. The voltmeter now reads the dc offset voltage. Adjust the pot closest to the test point to reduce the dc offset to 2 millivolts or less. Next place the channel select switch for that board in the up position. The RUN/RESET switch should be left in the RESET position. The D/A converter output is now at its maximum value. Adjust the gain pot to get a reading of 4.971 volts.

4.2 Setting the Internal Oscillator

The internal frequency reference is an oven stabilized crystal oscillator. Two adjustment points exist for this unit. The first is located within the oscillator itself. This one controls the oscillation frequency by adjusting the oven temperature. This adjustment has a wide range of tuning capability; however, with proper care, it can be used to set the operating frequency to within a part in 10^8. The second adjustment is via a 10-turn pot mounted on the front panel. The range of this adjustment is about 2 parts in 10^7.

The following procedure is suggested when adjusting the oscillator frequency.

1. Apply power to the oscillator and allow it to temperature stabilize for 20 to 30 minutes. The access plug located on top of the oscillator must be in place.

2. Synchronize an oscilloscope to an external 1 MHz reference and display the 1 MHz output. The display will appear to drift left if the oscillator frequency is higher than that of the reference and will drift to the right if it is lower than that of the reference. The rate of the drift indicates the relative frequency offset. One cycle in 1 second at 1 Mhz indicates an offset of 1 part in 10^6. If it takes 10 seconds to drift one cycle then the offset is 1 part in 10^7; 100 seconds to drift one cycle indicates an offset of 1 part in 10^8.

3. Position the 10-turn pot to its mid-range position and use the scope to estimate the frequency offset between the oscillator and the reference. If this offset is greater than about +-1 part in 10^7 then it will probably be necessary to make an initial adjustment of the oscillator oven.

4. To adjust the oven, remove the access screw and slightly rotate the adjustment screw inside the oscillator module. Rotating this screw clockwise lowers the oscillator frequency. Replace the access screw and allow 5 to 10 minutes for the oscillator to restabilize. After an adjustment the frequency increases slightly and then slowly comes down to the adjusted value.

   Using this procedure it is possible to set the oscillator to at least 1 part in 10^8 in about 30 to 40 minutes.

5. Once the oscillator has been brought into range via the oven adjustment, small tweak adjustments can be made using the 10 turn pot located on the front panel. Turn the pot clockwise to increase the oscillator frequency.

5. Internals

The generator contains five major subassemblies. These are:

Wire-Wrap panel.

This panel contains the sequence generators and timing circuitry for the four-hour schedule. It also provides the interconnections between the waveform generator boards, the front panel and the power supply. The panel is a 60-position AUGAT model 8136-PG21-60 panel.

Waveform Generator Boards

The input to these boards consists of a 1 MHz clock and a phase control signal. The 1 MHz clock is divided by a four digit BCD countdown. The output of the count down is then used to drive a divide-by-32 counter. The states of the divide-by-32 are used to address a read-only memory in which the samples of one period of a sine wave have been stored. The amplitudes of the samples are quantized to eight bits. The ROM outputs are gated to the D/A converter that generates the output waveform. The frequency of the output sinusoid is 1 MHz divided by 32 times the BCD divide factor.

A total of six waveformer boards were fashioned into a stack and were mounted next to the wire-wrap panel. The individual boards were connected to the wire-wrap panel using 16 conductor ribbon cables.

The board for channel 6 was modified by the addition of a pair of ROMS which were used to select between two possible divide factors.

Summer/Metering Board

This board accepts the outputs of the six level adjust pots and sums the signals to generate the output waveform. The circuitry used to generate the metering voltage is also contained on this board. The metering consisted of full wave rectifying the selected waveform and displaying the resulting average value. The metering is not true rms.

Oscillator

The oscillator is a VECTRON oven stabilized crystal oscillator set at a frequency of 16 MHz.

Power Supply

The power supply was to be a Semiconductor Circuits uninterrupible supply along with a 12-volt battery

pack. The UPS supplies did not arrive in time for inclusion. A Standard Power power supply was used instead. These units were purchased off the shelf at a local distributer.

The layout of the generator internals is shown in Figure 5.1. This figure is not drawn to scale.

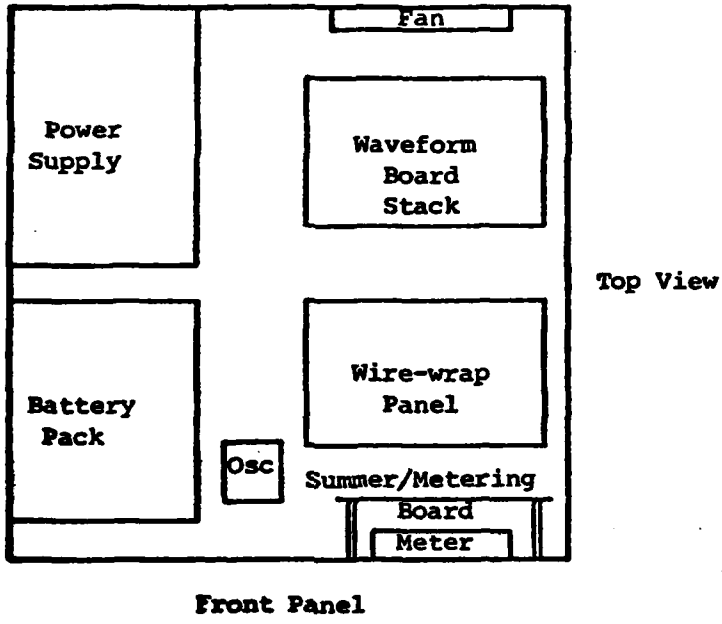


Figure 5.1. Generator internal component layout

5.1 Wire-Wrap Panel

This panel contains the circuitry needed to

1. distribute +5 and -5 volts to the waveform generator and summer/metering boards
2. implement the channel enable, run/reset and four-hour schedule functions
3. generate the required modulating sequences
4. route the analog output signals from the waveform generator boards to the level adjustment pots
5. divide the various possible clock frequencies to 1 MHz

The diagrams describing the wire-wrap panel logic are contained in Appendix A.

The wire-wrap panel contains three binary sequence generators.

The first is a ROM based generator that can be used to generate sequences containing as many as 32 digits. The number of carrier cycles per digit is hardwired to be 64. This number can be changed to values in the range of 1 thru 256, which are powers of 2, by moving one wire. In order to generate the PANOIC sequence the ROM contents are

Address	Contents
00	00100001
01	00000010
02	00000011
03	00100100
04	00000101
05	00100110
06	00100000

The low five bits select the next address to be read out of the ROM. The sixth bit from the right is the sequence bit used to generate the current digit. The top two bits are not used.

The second generator is used to generate the so-called WHAMMO signal. This is an augmented linear maximal sequence containing 512 digits. The setting on the BCSG-76 that will generate this sequence is 01257. The number of carrier cycles per digit is hardwired to be four. By changing one wire the number of cycles per digit can be set to 1, 2, 4, 8 or 16.

The third generator produces a 255-digit linear maximal sequence. The BCSG-76 setting corresponding to this sequence is 00455. The number of carrier cycles per digit is header selected and can be any value in the range of 1 thru 999.

The four-hour scheduler consists of a number of cascaded divide chains. First the 1 MHz clock is counted down by 10^8 in order to get a 0.01 Hz clock. This clock is divided by 12 to provide a clock that ticks every 20 minutes. The 20-minute period clock is divided by 12 in order to get a clock that has a four-hour period. The four-hour counter counts in 20-minute steps from 0 to 11. When the counter is in state 11, the waveform board outputs are turned off giving the quiet period. The counter goes from state 11 into state 0 on the next 20-minute tick.

External connections are made from the wire-wrap panel via cables listed below:

A01	channel 1 waveform board
B01	channel 2 waveform board
B02	channel 3 waveform board
B03	channel 4 waveform board
B04	channel 5 waveform boards
A27	connects power to the summer/metering board
A30	+-15 volt power supply

AJ1 channel selector switches
AJ2 level adjust potentiometers
BJ1 miscellaneous front panel functions

5.2 Waveformer Board Description

The organization of the waveform generator boards used in the SGEN79 generator is shown in Figure 5.2. (The reset logic is not included.) Appendix B contains the diagrams that describe the logic contained on these boards.

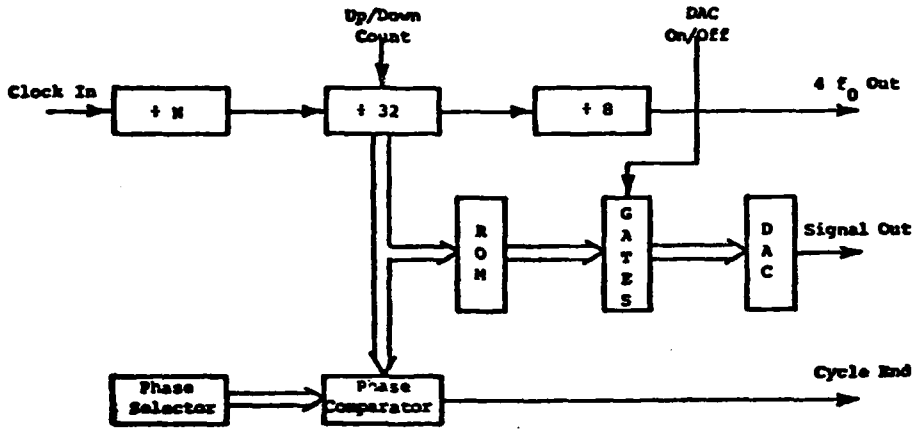


Figure 5.2. Waveformer board organization

The input clock is at a frequency of 1 MHz. This clock is divided using a four-digit BCD counter. The count factor is settable in the range from 1 thru 9999. The output of the BCD divider drives a divide-by-32.

The divide-by-32 is implemented using a binary up/down counter. The direction of count is determined by a logic signal originating off board. The five bits in the up/down counter are used to address a ROM. This ROM contains 32 8-bit samples of a sine wave. The counter also drives a comparator. When the count matches a preset value (set by a header or dip switch), a pulse is generated. This pulse can be used to drive off-board circuitry which counts carrier cycles and generates the up/down count enabling signal.

The clock used to drive the divide-by-32 is also used to drive a divide-by-8. The output of this counter is at four times the output sinusoid's carrier frequency. This feature was not used in the SGEN79 unit.

The ROM output is connected through a set of gates to the D/A converter. The gates are used to turn on and off the output without affecting the timing counts.

The contents of the sinusoid generating ROM are tabulated below.

Addr	Contents	Addr	Contents
00	01111111	20	10000001
01	01111101	21	10000011
02	01110101	22	10001011
03	01101010	23	10010110
04	01011010	24	10100110
05	01000111	25	10111001
06	00110001	26	11001111
07	00011001	27	11100111
10	00000000	30	00000000
11	11100111	31	00011001
12	11001111	32	00110001
13	10111001	33	01000111
14	10100110	34	01011010
15	10010110	35	01101010
16	10001011	36	01110101
17	10000011	37	01111101

The addresses are expressed as octal numbers and the contents as binary values.

5.2.1 Board Configuration

The waveform generator boards are assembled together into a stack. The stack is connected to the wire-wrap panel using six 16 wire cables. The signal assignments of the six boards are:

Bottom board

Signal channel 2, WHAMMO transmission. Modulation is CM. Connects to position B01 of the wire-wrap panel.

Board 2 from bottom

Signal channel 3, sequence transmission. Modulation is BM. Connects to position B02 of the wire-wrap panel.

Board 3 from bottom

Signal channel 4, CW signal. Connects to B03 of the wire-wrap panel.

Board 4 from bottom

Signal channel 5, CW signal. Connects to B04 of the wire-wrap panel.

Next to top board

Signal channel 6. CW signal. Divide factor selected out of a ROM using a front panel switch. Connects to B05 of the wire-wrap panel.

Top Board

Signal channel 1. PANOIC signal. Modulation is CM. Connects to A01 of the wire-wrap panel.

5.2.2 Headers

The clock divide factor settings are determined by the presence and absence of jumper wires mounted on headers. The presence of a wire represents a logical 0 and the absence represents a logical 1. The divide factors are expressed as BCD numbers. The divide factor can range from 1 thru 9999. Two headers are used to set the divide factor. Each header corresponds to two BCD digits of information. In the examples below the divide factors read from bottom (most significant digit) to top (least significant digit).

divide by 210	divide by 138	divide by 574
1----16	1----16	1----16
2----15	2----15	2----15
3----14	3----14	3 14
4----13	4 13	4----13
5 12	5 12	5 12
6----11	6 11	6 11
7----10	7----10	7 10
8---- 9	8---- 9	8---- 9
1----16	1 16	1 16
2 15	2----15	2----15
3----14	3----14	3 14
4----13	4----13	4----13
5----12	5----12	5----12
6----11	6----11	6----11
7----10	7----10	7----10
8---- 9	8---- 9	8---- 9

The modulation angle is set using wire jumpers mounted on a single dip header. The presence of a wire indicates a logical 1 and the absence of a wire indicates a logical 0.

CM mod	BM mod
1 16	1 16
2 15	2 15
3 14	3 14
4 13	4 13
5 12	5 12
6----11	6 11
7 10	7----10
8 9	8 9

5.3 Summer/Metering Board

The summer/metering board is built on a piece of perf board which is mounted on the back of the SGEN79 front panel. Time did not allow having a proper printed circuit board made for this circuit. The board was mounted on the back of the front panel in an attempt to minimize crosstalk between the analog and digital parts of the generator. This attempt was largely successful. Appendix C contains the diagrams describing the circuits contained on this board.

The D/A converter outputs of the waveform boards are connected to the level adjust pots located on the front panel. The wipers on these pots feed unity gain buffer amplifiers on the metering board. The buffers are used to provide low impedance signals which isolate the pot settings from loading by the summer amplifier and the metering circuitry. These amplifiers were probably unnecessary.

The buffer amplifier outputs are summed together using an inverting "amplifier" with a gain of 1/5. This value of gain allowed the outputs of the 6 channels to be summed without having to worry about the output amplifier clipping. The output of the summer amplifier is buffered using a complementary symmetric pair of transistors inside of the feedback loop.

The buffer outputs are also connected to a rotary switch that is used to select channels for metering. A gain of 1/5 is used in the metering circuitry when one of the individual channels is to be metered. This was done to place the same gain on the individual channels as on the summed waveform.

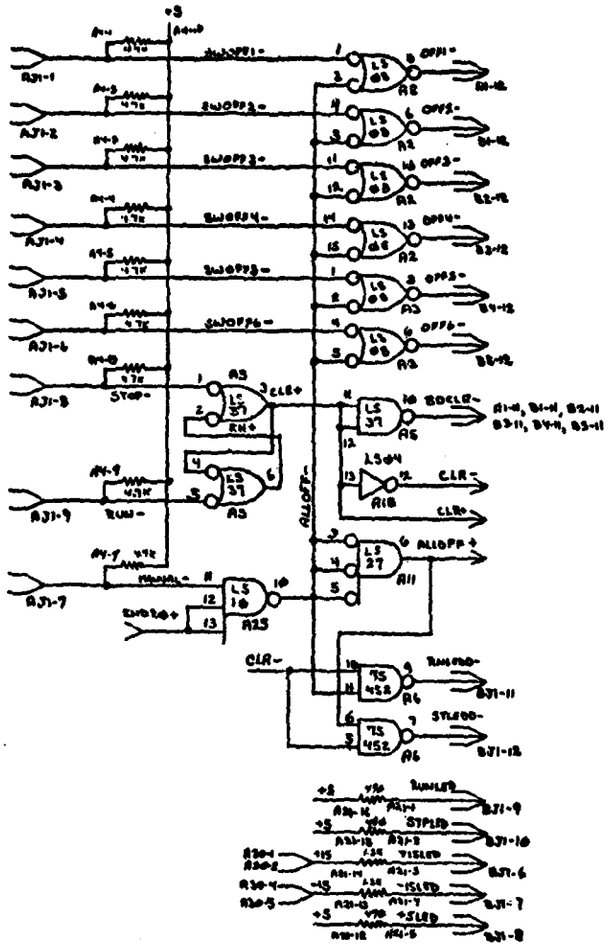
The waveform selected for metering drives a unity gain amplifier when using the millivolt range and a gain of 1/10 amplifier when using the volt range. The meter amplifier output is ac coupled into a full wave rectifier. The output of the rectifier is low pass filtered with the resulting output driving an Analog Devices digital panel meter. The low pass filter was implemented using a Sellin-Key two-pole low pass configuration with a nominal cut-off frequency of 2 Hz.

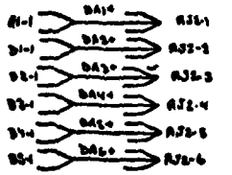
The National Semiconductor LM308A op amp was used throughout this circuit because of its low offset voltage, low bias current and excellent stability properties.

Connections to the summer/metering board are:

A2	power from wire-wrap panel position A27
A3	driver transistors, output signal, meter connections
E1	channel metering rotary selector switch
E2	channel metering rotary selector switch
E3	level adjust potentiometer wipers

Appendix A: Wire-Wrap Panel Diagrams

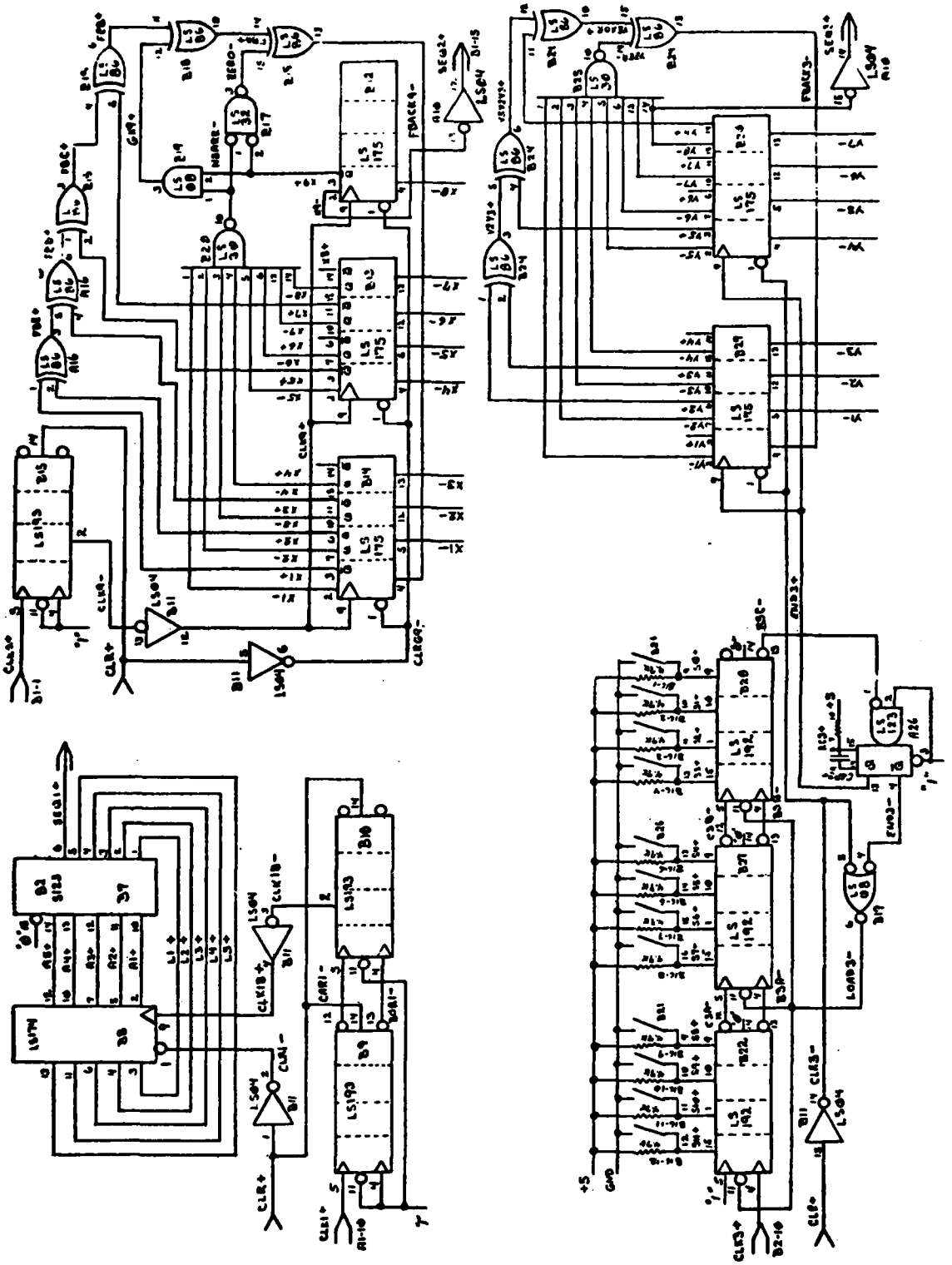


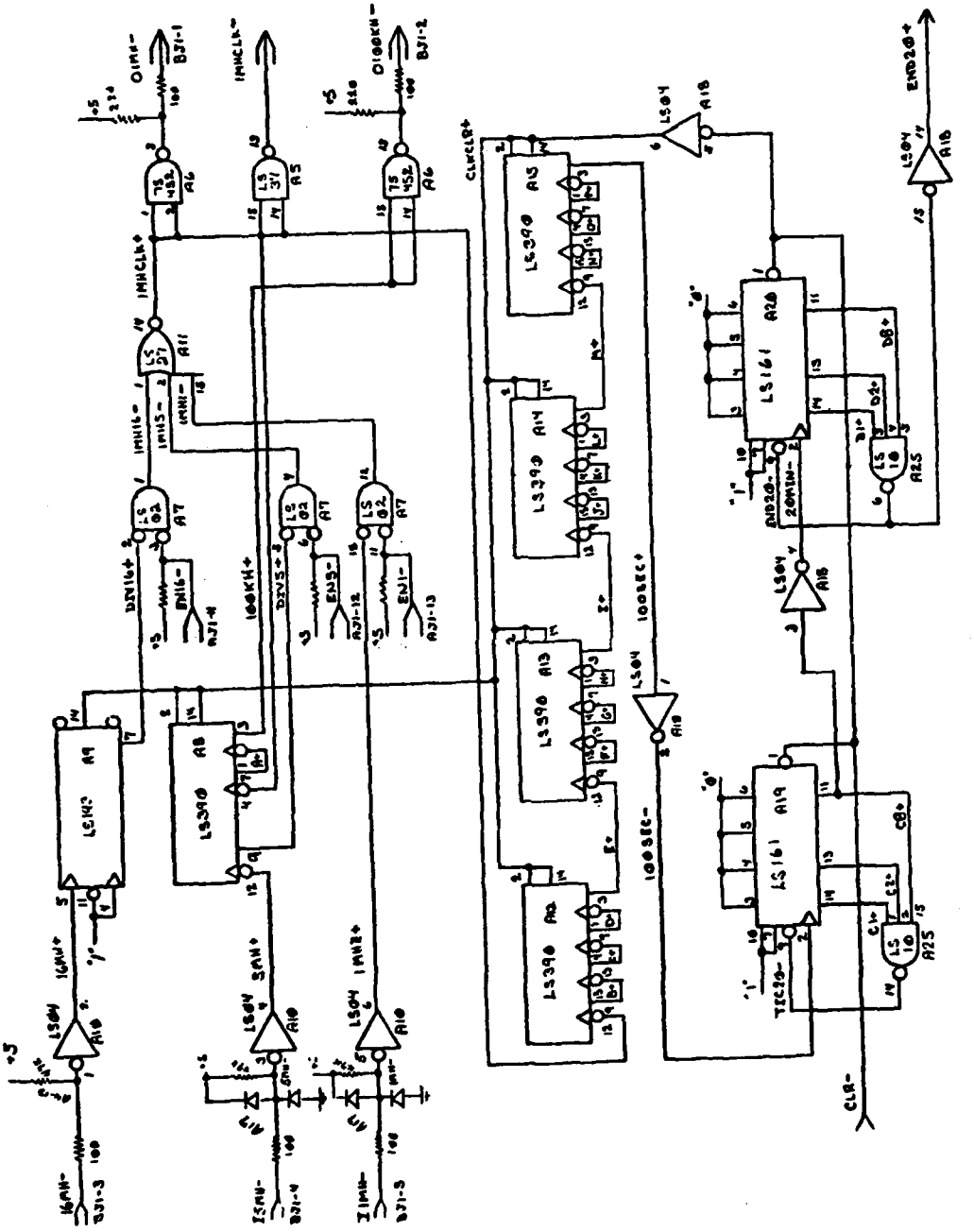


WAVEFORMER BOARDS TO LEVEL ADJUST POTS

*5 ALSO CONNECTED TO A1-8, B1-2, B2-2, B3-2, B4-2, B5-2, A27-2, A32-9
*15 ALSO CONNECTED TO A1-1, B1-3, B2-3, B3-3, B4-3, B5-3, A28-10, A27-3

THIS PAGE IS BEST QUALITY PRACTICABLE





A 1

17-H0018	0-L0098
16-H0019	1-BA1*
15-SR01*	2-*15
14-L0099	3--15
13-	4-L0038
12-OPP1-	5-L0093
11-BRCLR-	6-L0078
10-CLR1*	7-L0098
9-1MHCLK-	8-L0088

HEADER

A 2

17-H0023	0-L0018
16-H0028	1-SWOPP1-
15-ALLOPP-	2-ALLOPP-
14-SWOPP4-	3-OPP1-
13-OPP4-	4-SWOPP2-
12-ALLOPP-	5-ALLOPP-
11-SWOPP3-	6-OPP2-
10-OPP3-	7-L0018
9-	8-

7408

A 3

17-H0038	0-L0028
16-H0038	1-SWOPP5-
15-	2-ALLOPP-
14-	3-OPP5-
13-	4-SWOPP6-
12-	5-ALLOPP-
11-	6-OPP6-
10-	7-L0028
9-	8-

7408

A 4

17-H0048	0-L0038
16-H0048	1-SWOPP1-
15-ASIGNL-	2-SWOPP2-
14-	3-SWOPP3-
13-16MH-	4-SWOPP4-
12-SN1-	5-SWOPP5-
11-EN5-	6-SWOPP6-
10-2N16-	7-MANUAL-
9-RUN-	9-STOP-

RESNET

A 5

17-H0058	0-L0048
16-H0058	1-STOP-
15-1MHCLK*	2-RN*
14-1MHCLK*	3-CLR*
13-1MHCLK-	4-CLR*
12-CLR*	5-RUN-
11-CLR*	6-RN*
10-BRCLR-	7-L0048
9-	8-

7437

A 6

17-H0068	0-L0108
16-H0068	1-1MHCLK*
15-100KH*	2-1MHCLK*
14-100KH*	3-01MH-
13-0100KH-	4-L0108
12-H0068	5-CLR-
11-ALLOPP-	6-ALLOPP*
10-CLR-	7-STL200-
9-RNL200-	8-L0108

75452

A 7

17-H0078	0-L0118
16-H0078	1-1MH16-
15-	2-DIV16*
14-	3-EN16-
13-	4-1MH5-
12-1MH1-	5-DIV5*
11-EN1-	6-EN5-
10-1MHZ*	7-L0118
9-	8-

7402

A 8

17-H0088	0-L0128
16-H0088	1-A*
15-	2-CLKCLR*
14-CLKCLR*	3-100KH*
13-	4-1MHCLK*
12-5MH*	5-
11-	6-
10-	7-A*
9-DIV5*	8-L0128

74390

A 9

17-H0098	0-L0138
16-H0098	1-
15-	2-
14-CLKCLR*	3-
13-	4-H0098
12-	5-16MH*
11-H0098	6-
10-	7-DIV16*
9-	8-L0138

74193

A10

17-H0108	0-L0148
16-H0108	1-16MH-
15-X8-	2-16MH*
14-SEQ3*	3-5MH-
13-X9-	4-5MH*
12-SEQ2*	5-1MH-
11-	6-1MHZ*
10-	7-L0148
9-	8-

7404

A11

17-H0118	0-L0158
16-H0118	1-1MH16-
15-1MH1-	2-1MH5-
14-1MHCLK*	3-ALLOPP-
13-	4-ALLOPP-
12-	5-ALLOPP-
11-	6-ALLOPP*
10-	7-L0158
9-	8-

7427

A12

17-H0128	0-L0168
16-H0128	1-D*
15-B*	2-CLKCLR*
14-CLKCLR*	3-B*
13-C*	4-C*
12-1MHCLR*	5-
11-	6-
10-	7-D*
9-B*	8-L0168

74390

A13

17-H0138	0-L0178
16-H0138	1-R*
15-F*	2-CLKCLR*
14-CLKCLR*	3-I*
13-G*	4-G*
12-E*	5-
11-	6-
10-	7-H*
9-F*	8-L0178

74390

A14

17-H0148	0-L0188
16-H0148	1-L*
15-J*	2-CLKCLR*
14-CLKCLR*	3-N*
13-K*	4-K*
12-I*	5-
11-	6-
10-	7-L*
9-J*	8-L0188

74390

A15

17-H0158	0-L0198
16-H0158	1-P*
15-M*	2-CLKCLR*
14-CLKCLR*	3-100SEC*
13-O*	4-O*
12-M*	5-
11-	6-
10-	7-P*
9-N*	8-L0198

74390

A16

17-H0216	0-L0209
16-H0216	1-X1↓
15-	2-X2↓
14-	3-PBP↓
13-	4-Y1↓
12-	5-PBP↓
11-	6-PBD↓
10-	7-L0209
9-	8-

7486

A17

17-H0178	0-L0218
16-SMH-	1-ISMH-
15-SMH-	2-L0218
14-SMH-	3-H0178
13-SMH-	4-H0178
12-1MH-	5-I1MH-
11-1MH-	6-L0218
10-1MH-	7-H0178
9-1MH-	8-H0178

HEADER

A18

17-H0188	0-L0228
16-H0188	1-100SEC↓
15-END20-	2-100SEC-
14-END20↓	3-C8↓
13-CLR↓	4-20MIN-
12-CLR-	5-CLR-
11-	6-CLKCLR↓
10-	7-L0228
9-	8-

7404

A19

17-H0198	0-L0238
16-H0198	1-CLR-
15-	2-100SEC-
14-C1↓	3-L0238
13-C2↓	4-L0238
12-	5-L0238
11-C8↓	6-L0238
10-H0198	7-H0198
9-TIC20-	8-L0238

74161

A20

17-H0208	0-L0248
16-H0208	1-CLR-
15-	2-20MIN-
14-D1↓	3-L0248
13-D2↓	4-L0248
12-	5-L0248
11-D8↓	6-L0248
10-H0208	7-H0208
9-END20-	8-L0248

74161

A21

17-H0218	0-
16-H0218	1-RDWLRD
15-H0218	2-STPLRD
14-↓15	3-↓15LRD
13--15	4--15LRD
12-H0218	5-↓5LRD
11-	6-
10-H0218	7-RC1↓
9-CAP1↓	8-RC1↓

HEADER

A22

17-H0228	0-
16-H0228	1-01MH-
15-H0228	2-0100KH-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

HEADER

A23

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

A24

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

A25

17-H0238	0-L0258
16-H0238	1-C1↓
15-C8↓	2-C2↓
14-TIC20-	3-D1↓
13-END20↓	4-D2↓
12-END20↓	5-D8↓
11-MANUAL-	6-END20-
10-ALLOFF-	7-L0258
9-	8-

7410

A26

17-H0248	0-L0268
16-H0248	1-B3C-
15-RC1↓	2-H0248
14-CAP3↓	3-H0748
13-PWD1↓	4-PWD1-
12-	5-
11-	6-
10-	7-
9-	8-L0268

74123

A27

17-H0258	0-L0278
16-H0258	1-
15-	2-↓15
14-	3--15
13-	4-L0278
12-	5-L0278
11-	6-L0278
10-	7-L0278
9-	8-L0278

HEADER

A28

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

A29

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

A30

17-	0-L0288
16-L0288	1-↓15
15-L0288	2-↓15
14-	3-
13-L0288	4--15
12-L0288	5--15
11-	6-
10-	7-
9-	8-

HEADER

AJ1	AJ2
1-SWOPP1-	1-DA1+
2-SWOPP2-	2-DA2+
3-SWOPP3-	3-DA3+
4-SWOPP4-	4-DA4+
5-SWOPP5-	5-DA5+
6-SWOPP6-	6-DA6+
7-MANUAL-	7-
8-STOP-	8-
9-RUN-	9-
10-ASIGNL-	10-
11-PW15-	11-
12-LN5-	12-
13-PW1-	13-
14-LOGIC	14-LOGIC
15-LOGIC	15-LOGIC
16-LOGIC	16-LOGIC
17-LOGIC	17-LOGIC
18-LOGIC	18-LOGIC
19-LOGIC	19-LOGIC
20-LOGIC	20-
21-LOGIC	21-
22-LOGIC	22-
23-LOGIC	23-
24-LOGIC	24-
25-LOGIC	25-
26-LOGIC	26-

B 1

17-H0296	0-L0299
16-H0296	1-DA2+
15-	2-+15
14-L0298	3--15
13-	4-L0299
12-OFF2-	5-L0298
11-BDCLR-	6-L0299
10-CLK2+	7-L0298
9-INHCLR-	8-L0298

HEADER

B 2

17-H0297	0-L0058
16-H0297	1-DA3+
15-H0293	2-+15
14-L0058	3--15
13-	4-L0058
12-OFF3-	5-L0058
11-BDCLR-	6-L0058
10-CLK3+	7-L0058
9-INHCLR-	8-L0058

HEADER

B 3

17-H0288	0-L0068
16-H0288	1-DA4+
15-	2-+15
14-L0068	3--15
13-	4-L0068
12-OFF4-	5-L0068
11-BDCLR-	6-L0068
10-	7-L0068
9-INHCLK-	8-L0068

HEADER

B 4

17-H0298	0-L0078
16-H0298	1-DA5+
15-	2-+15
14-L0078	3--15
13-	4-L0078
12-OFF5-	5-L0078
11-BDCLR-	6-L0078
10-	7-L0078
9-INHCLK-	8-L0078

HEADER

B 5

17-H0309	0-L0098
16-H0309	1-DA6+
15-	2-+15
14-ASIGNL-	3--15
13-	4-L0088
12-OFF6-	5-L0088
11-BDCLR-	6-L0088
10-	7-L0088
9-INHCLK-	8-L0088

HEADER

B 6

17-H0318	0-
16-H0318	1-L1+
15-	2-L2+
14-	3-L3+
13-	4-L4+
12-	5-L5+
11-	6-
10-	7-
9-	8-

RESET

B 7

17-H0328	0-L0308
16-H0328	1-L1+
15-L0308	2-L2+
14-A5+	3-L3+
13-A4+	4-L4+
12-A3+	5-L5+
11-A2+	6-SEW1+
10-A1+	7-
9-	8-L0308

8223

B 8

17-H0338	0-L0318
16-H0339	1-CLR1-
15-	2-A1+
14-	3-L1+
13-L5+	4-L2+
12-A5+	5-A2+
11-L4+	6-L3+
10-A4+	7-A3+
9-CLK1B+	8-L0318

74174

B 9

17-H0348	0-L0328
16-H0348	1-
15-	2-
14-CLR+	3-
13-DOR1-	4-H0348
12-CAR1-	5-CLK1+
11-H0348	6-
10-	7-
9-	8-L0328

74193

B10

17-H0358	0-L0338
16-H0358	1-
15-	2-CLK1B-
14-CLR+	3-
13-	4-BOR1-
12-	5-CAR1-
11-H0358	6-
10-	7-
9-	8-L0338

74193

B11

17-H0368	0-L0348
16-H0368	1-CLR+
15-CLR+	2-CLR1-
14-CLR1-	3-CLK1B-
13-CLK9-	4-CLK10+
12-CLK9+	5-CLP+
11-	6-CLRG9-
10-	7-L0348
9-	8-

7404

B12

17-H0378	0-L0358
16-H0378	1-CLRG9-
15-	2-X8-
14-	3-X8+
13-	4-X8-
12-	5-
11-	6-
10-	7-
9-CLK9+	8-L0358

74175

B13

17-H0388	0-L0368
16-H0388	1-CLRG9-
15-X8-	2-X5-
14-X8+	3-X5+
13-X7-	4-X8-
12-X6-	5-X5-
11-X7+	6-X6+
10-X7-	7-X6-
9-CLK9+	8-L0368

74175

B14

17-H0398	0-L0378
16-H0398	1-CLRG9-
15-X4-	2-X1-
14-X4+	3-X1+
13-X3-	4-FBACK9-
12-X2-	5-X1-
11-X3+	6-X2+
10-X3-	7-X2-
9-CLK9+	8-L0378

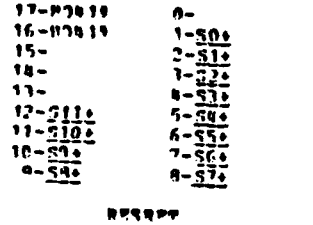
74175

B15

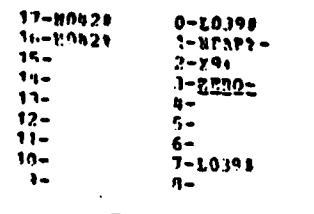
17-H0408	0-L0388
16-H0408	1-
15-	2-CLK2-
14-CLR+	3-
13-	4-H0408
12-	5-CLK2+
11-H0408	6-
10-	7-
9-	8-L0388

74193

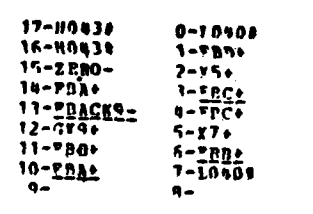
B16



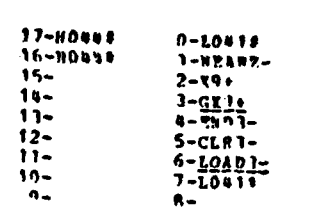
B17



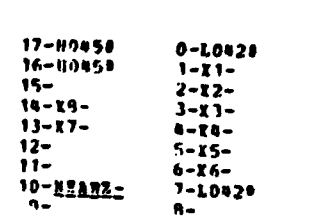
B18



B19



B20



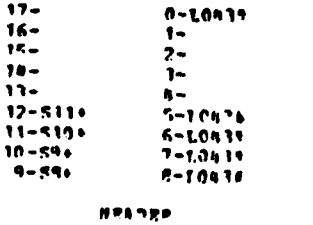
7832

7806

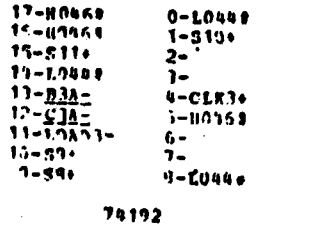
7808

7830

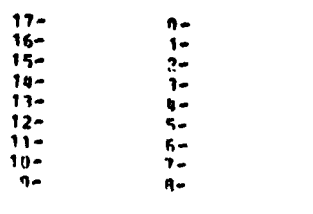
B21



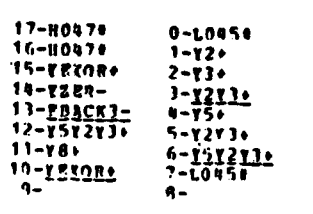
B22



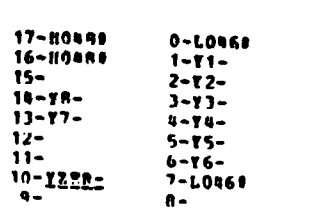
B23



B24



B25

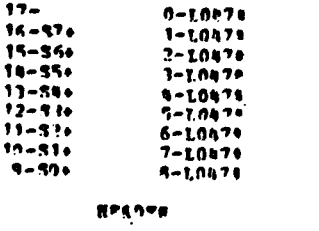


74192

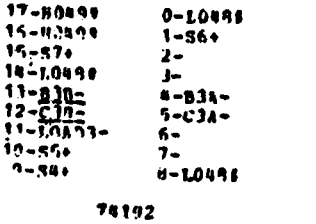
7806

7830

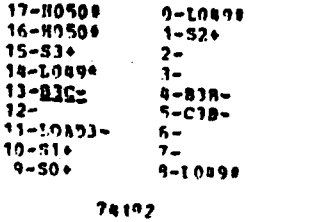
B26



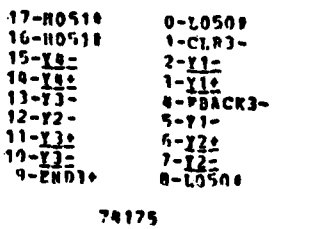
B27



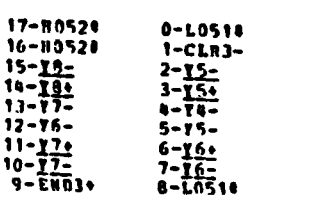
B28



B29



B30

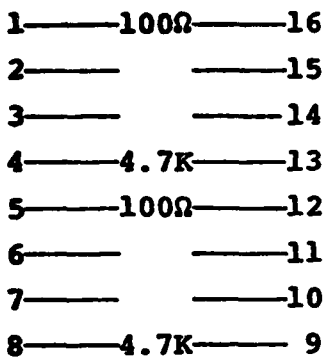


74192

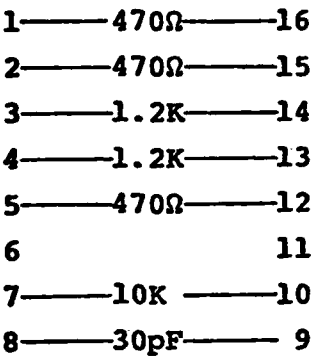
74175

74175

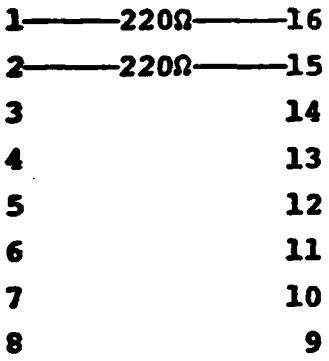
PJ1	PJ2
1-0198-	1-
2-0100KH-	2-
3-16KH-	3-
4-15KH-	4-
5-11KH-	5-
6-+15LPB	6-
7--15LPB	7-
8-+5LPB	8-
9-PUSLPB	9-
10-STPLPB	10-
11-PULPBB-	11-
12-STLPBB-	12-
13-	13-
14-L0059	14-
15-L0059	15-
16-L0059	16-
17-L0059	17-
18-L0060	18-
19-L0060	19-
20-L0060	20-
21-L0060	21-
22-L0070	22-
23-L0070	23-
24-L0070	24-
25-L0070	25-
26-L0040	26-


1 100Ω 16
2 15
3 14
4 4.7K 13
5 100Ω 12
6 11
7 10
8 4.7K 9

A17


1 470Ω 16
2 470Ω 15
3 1.2K 14
4 1.2K 13
5 470Ω 12
6 11
7 10K 10
8 30pF 9

A21

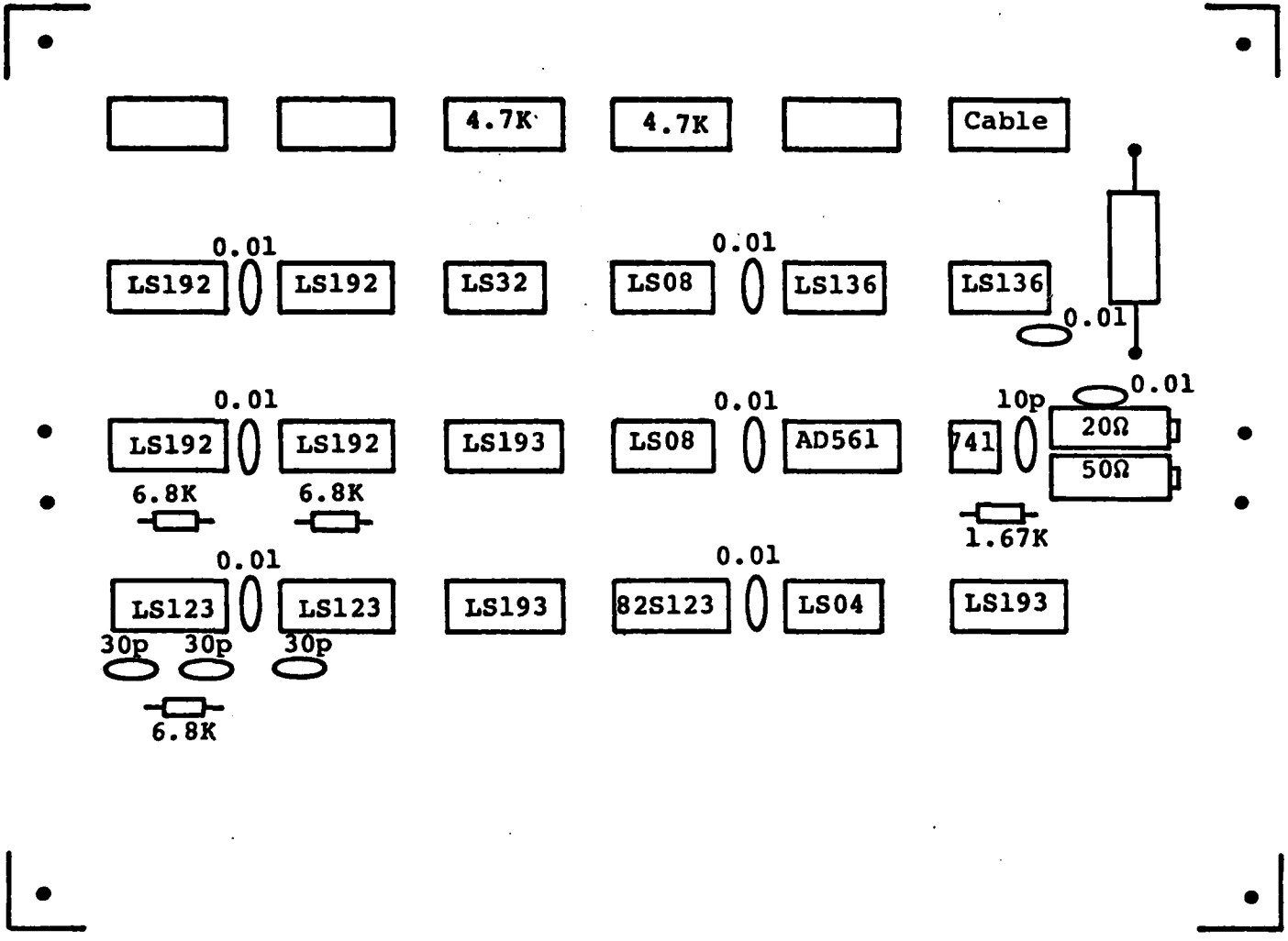

1 220Ω 16
2 220Ω 15
3 14
4 13
5 12
6 11
7 10
8 9

A23

Appendix B: Waveformer Board Diagrams

I/O Connector pin assignments:

1	DAC output
2	+15 volts input
3	-15 volts input
4	ground
5	ground
6	ground
7	ground
8	ground
9	1 MHz clock input
10	cycle end pulse output
11	clear- input
12	output enable+ input
13	4 times carrier clock output
14	ground
15	digit phase select input
16	+5 volts input



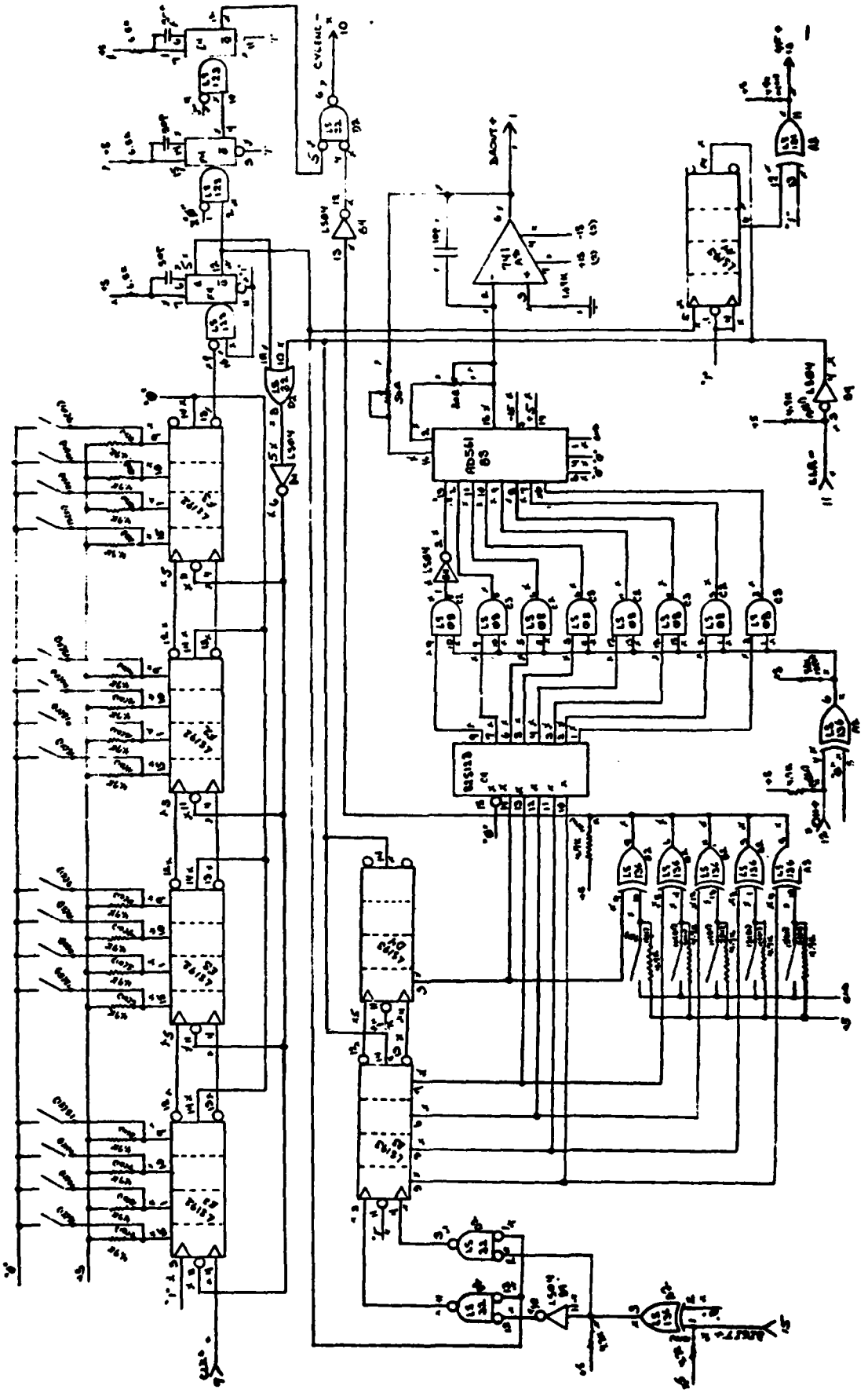
Waveform generator IC placement

Modified Waveformer Board

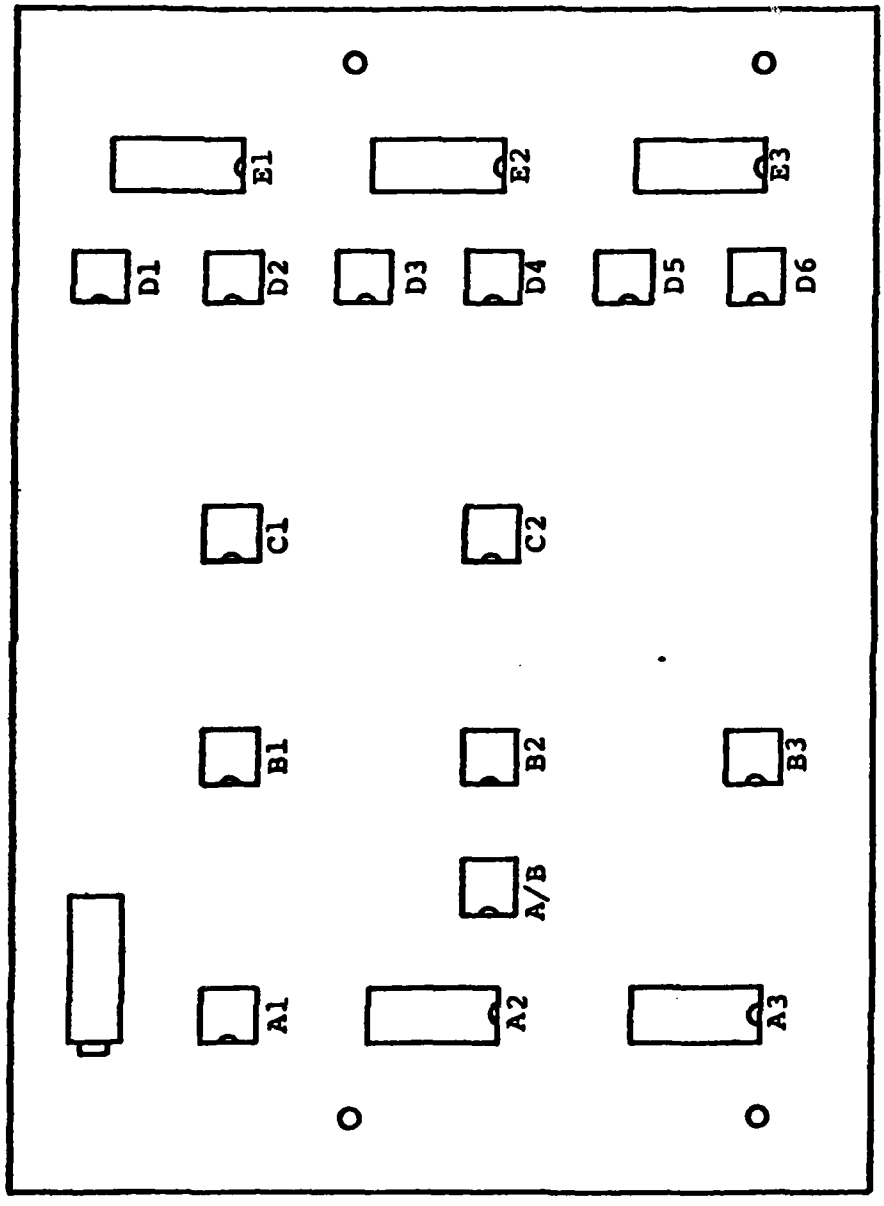
One waveformer board was modified by adding two 82S23 ROMs and two dip sockets for cable connections. The ground was removed from pin 14 of the I/O socket. Pin 14 was then jumpered to pin 10 of the two ROMs. Pin 14 was used to select one of two control words programmed into the ROMs that were to select the divide count.

The eight open collector outputs of each ROM were wired to a dip socket. These sockets were positioned so that a short jumper cable allowed ready connection between a given socket and one of the two sockets provided for setting the BCD divide digits. Pin assignments were chosen to allow the ROM outputs to set the divide factor. The pin assignments used on each ROM were:

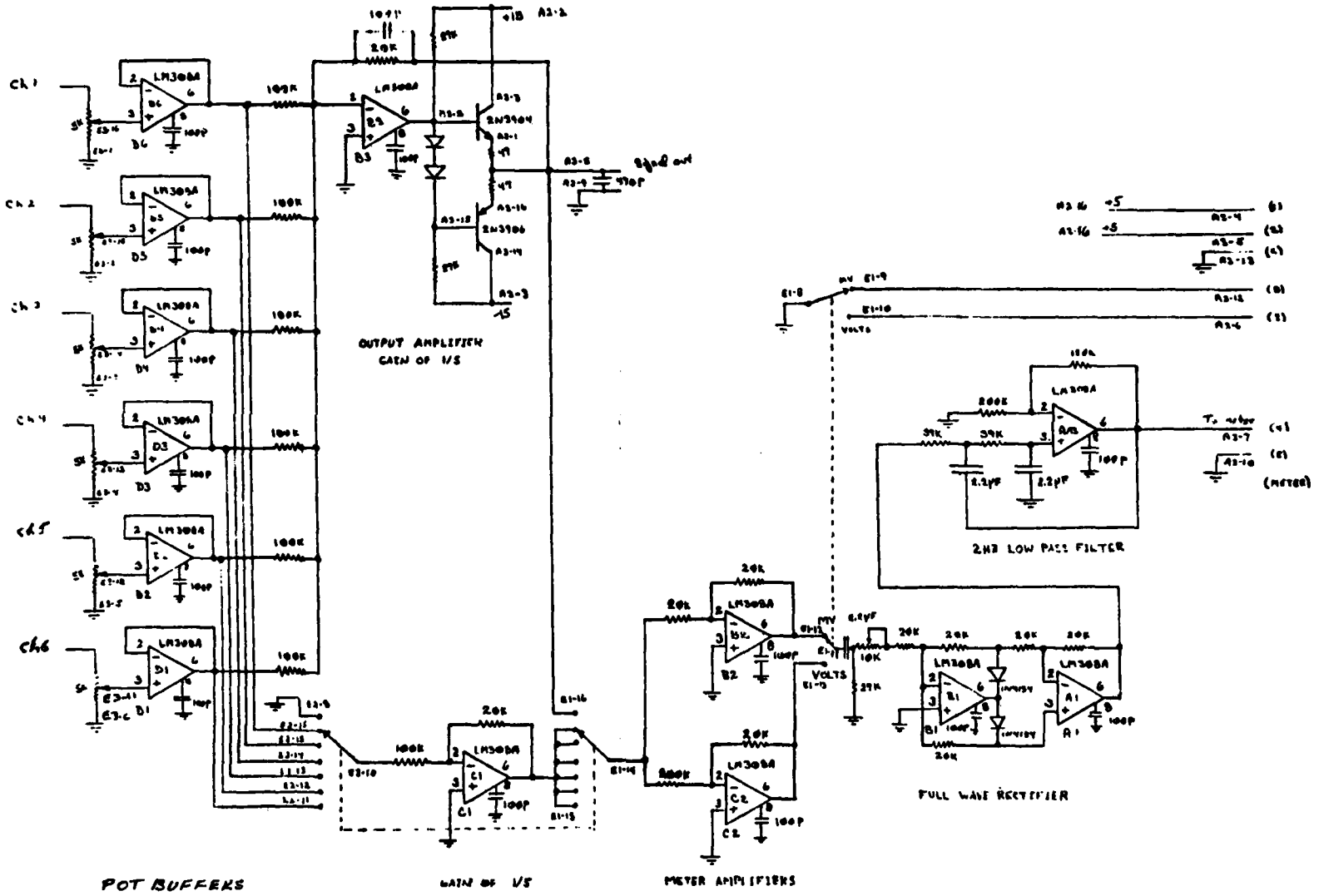
1 cable pin 16	16 +5 volts
2 cable pin 15	15 ground
3 cable pin 14	14 ground
4 cable pin 13	13 ground
5 cable pin 12	12 ground
6 cable pin 11	11 ground
7 cable pin 10	10 ground
8 ground	9 cable pin 9



Appendix C: Summer/Metering Board Diagrams



Analog Mixer Board
(Component Side)


Ch 1
Ch 2
Ch 3
Ch 4
ch5
ch6
LM308A
100K
100P
+15
2N3904
2N3906
OUTPUT AMPLIFIER
GAIN OF 1/5
20K
200K
39K
2.2μF
10K
VOLTS
2nd LOW PASS FILTER
FULL WAVE RECTIFIER
POT BUFFERS
GAIN OF 1/5
METER AMPLIFIERS

Appendix D: Cable Pin Assignments

Wire-wrap Panel Connector AJ1

Pin	Connection
1	Channel 1 toggle switch top lug
2	Channel 2 toggle switch top lug
3	Channel 3 toggle switch top lug
4	Channel 4 toggle switch top lug
5	Channel 5 toggle switch top lug
6	Channel 6 toggle switch top lug
7	No connection (contains MANUAL-)
8	Reset toggle switch top lug and external reset BNC center
9	Reset toggle switch bottom lug
10	A - B selector toggle switch meter side lug
11	Clock selector rotary switch INT position
12	Clock selector rotary switch 5MHz position
13	Clock selector rotary switch 1 MHz position
14	Channel 1 toggle switch center lug
15	Channel 2 toggle switch center lug
16	Channel 3 toggle switch center lug
17	Channel 4 toggle switch center lug
18	Channel 5 toggle switch center lug
19	Channel 6 toggle switch center lug
20	No connection (contains ground)
21	Reset toggle switch center lug and reset BNC grounding lug
22	Reset toggle switch center lug
23	A - B selector toggle switch center lug
24	Common terminal on clock selector rotary switch
25	Common terminal on clock selector rotary switch
26	Common terminal on clock selector rotary switch

Wire-wrap Panel Connector AJ2

Pin	Connection
1	Channel 1 level adjust pot, lug closest to panel
2	Channel 2 level adjust pot, lug closest to panel
3	Channel 3 level adjust pot, lug closest to panel
4	Channel 4 level adjust pot, lug closest to panel
5	Channel 5 level adjust pot, lug closest to panel
6	Channel 6 level adjust pot, lug closest to panel
7	free
8	free
9	free
10	free
11	free
12	free
13	free
14	Channel 1 level adjust pot, back lug (non wiper)
15	Channel 2 level adjust pot, back lug (non wiper)
16	Channel 3 level adjust pot, back lug (non wiper)
17	Channel 4 level adjust pot, back lug (non wiper)

18	Channel 5 level adjust pot, back lug (non wiper)
19	Channel 6 level adjust pot, back lug (non wiper)
20	free
21	free
22	free
23	free
24	free
25	free
26	free

Wire-wrap Panel Connector BJ1

Pin	Connection
1	1 MHz clock output BNC center pin thru 100 ohms
2	100 KHz clock output BNC center pin thru 100 ohms
3	Vectron oscillator clock output pin 1
4	5 MHz clock input BNC center pin
5	1 MHz clock input BNC center pin
6	Anode of +15 LED
7	Cathode of -15 LED
8	Anode of +5 LED
9	Anode of ACTIVE LED
10	Anode of QUIET LED
11	Cathode of ACTIVE LED
12	Cathode of QUIET LED
13	free
14	1 MHz clock output BNC ground lug
15	100 KHz clock output BNC ground lug
16	Vectron oscillator pin 5
17	5 MHz clock input ground lug
18	1 MHz clock input ground lug
19	Cathode of +15 LED
20	Anode of -15 LED
21	Cathode of +5 LED
22	No connection (contains ground)
23	No connection (contains ground)
24	No connection (contains ground)
25	No connection (contains ground)
26	No connection (contains ground)

Adder/Meter Board Connector A2

Pin	Position
1	free
2	+15 volts
3	-15 volts
4	ground
5	ground
6	ground
7	ground
8	ground
9	free
10	free

11	free
12	free
13	free
14	free
15	free
16	+5 volts

Note: This is a ribbon cable that connects to the wire-wrap panel at position A27.

Adder/Meter Board Connector A3

Pin	Connection
1	Emitter of 2N3904 (NPN)
2	Base of 2N3904
3	Collector of 2N3904 (also +15 volts)
4	Meter pin 1
5	Meter pin 2
6	Meter pin 3
7	Meter pin 4
8	Both signal output BNC connectors, center pin
9	Both signal output BNC connectors, ground lug
10	Meter pin E
11	free
12	Meter pin B
13	Meter pin C
14	Collector of 2N3906 (also -15 volts)
15	Base of 2N3906
16	Emitter of 2N3906 (PNP)

Adder/Meter Board Connector E1

Pin	Connection
1	No connection (contains ground)
2	No connection (contains ground)
3	No connection (contains ground)
4	No connection (contains ground)
5	No connection (contains ground)
6	No connection (contains ground)
7	No connection (contains ground)
8	Center of Volt/MV switch, pole 2
9	Pot side of Volt/MV switch, pole 2
10	Meter side of Volt/MV switch, pole 2
11	Center of Volt/MV switch, pole 1
12	Pot side of Volt/MV switch, pole 1
13	Meter side of Volt/MV switch, pole 1
14	Meter select rotary switch wiper, pole 1
15	Meter select rotary switch positions 1-6, pole 1
16	Meter select rotary switch position 0, pole 1

Adder/Meter Board Connector E2

Pin	Connection
1	No connection (contains ground)
2	No connection (contains ground)
3	No connection (contains ground)
4	No connection (contains ground)
5	No connection (contains ground)
6	No connection (contains ground)
7	No connection (contains ground)
8	Meter select rotary switch position 0, pole 2
9	free
10	Meter select rotary switch wiper, pole 2
11	Meter select rotary switch position 6, pole 2
12	Meter select rotary switch position 5, pole 2
13	Meter select rotary switch position 4, pole 2
14	Meter select rotary switch position 3, pole 2
15	Meter select rotary switch position 2, pole 2
16	Meter select rotary switch position 1, pole 2

Adder/Meter Board Connector E3

Pin	Connection
1	Channel 1 level adjust pot, back lug (non wiper)
2	Channel 2 level adjust pot, back lug (non wiper)
3	Channel 3 level adjust pot, back lug (non wiper)
4	Channel 4 level adjust pot, back lug (non wiper)
5	Channel 5 level adjust pot, back lug (non wiper)
6	Channel 6 level adjust pot, back lug (non wiper)
7	No connection (contains ground)
8	No connection (contains ground)
9	free
10	free
11	Channel 6 level adjust pot, wiper
12	Channel 5 level adjust pot, wiper
13	Channel 4 level adjust pot, wiper
14	Channel 3 level adjust pot, wiper
15	Channel 2 level adjust pot, wiper
16	Channel 1 level adjust pot, wiper

Vectron Oscillator Connector

Pin	Connection
1	Goes to BJ1 pin 3 on wire wrap panel
2	Connect to pin 3 on this connector thru 100 ohms
3	Connect to pin 2 and logic power ground
4	Connect to +5 logic supply
5	Goes to BJ1 pin 16 on wire wrap panel
6	20K frequency adjust pot, lug close to front panel
7	20K frequency adjust pot, wiper lug
8	20K frequency adjust pot, lug at back

Appendix E: Data Sheets

This appendix contains the following data sheets:

Analog Devices AD2026 Digital Panel Meter

Analog Devices AD561 10 bit Monolithic D/A Converter

National Semiconductor LM308A Operational Amplifier

National Semiconductor LM741 Operational Amplifier

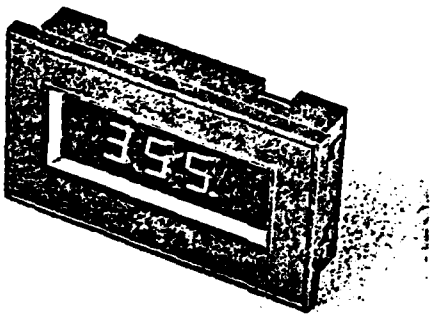
Vectron Laboratories CO211 Oven Stabilized Oscillator

ANALOG DEVICES

Low Cost 3 Digit Analog Panel Meter Replacement

AD2026*

FEATURES
Third Generation I^2L LSI Design
Small Size and Weight: 3.4"W x 2.0"H x 0.8"D; 1.8 Ounces
Snap-In Mounting, No Hardware Required
Low Power: +5V at 0.6 Watts
Balanced Differential Input
High Reliability: >250,000 Hour MTBF
Low Cost: $34 in 100s
$29 in 1000s



GENERAL DESCRIPTION
The AD2026 is specifically designed to provide a digital alternative to analog panel meters. Most of the analog and digital circuitry is implemented on a single proprietary I^2L LSI chip. Only 13 additional electrical components are required. The complete DPM is mounted on a single 3" x 1 5/8" PCB. A unique case design (patent applied for) utilizes molded-in fingers, both to capture the PCB in the case and to provide snap-in mounting of the DPM in a standard panel cutout. No mounting hardware of any kind is used. The DPM occupies less than 1" of space behind the panel.

EXCELLENT PERFORMANCE
The AD2026 is not a conventional DPM stripped down to achieve a low price. It offers the instrument designer digital accuracy, resolution and ease of readout, while occupying less volume than its analog counterpart. Other features of analog meters, such as reliability and instantaneous operation, are retained in the AD2026. Features usually not required in displaying measurement results in instruments, such as full bipolar input, 100% overrange, rejection of normal mode signals, and true auto zero, have been eliminated to achieve a reliable, yet low cost design.

The AD2026 measures and displays inputs from -99mV to +999mV, with an accuracy of 0.1% of reading ±1 digit. Zero shift is less than one bit over the full operating temperature range, resulting in the same performance as a DPM with auto zero. The balanced differential input rejects common mode voltages up to 200mV, enough to eliminate most ground loop problems.

Automatic polarity indication is provided by using the third digit to indicate negative inputs. Automatic overrange indication for inputs greater than +999mV is displayed as FEE, and for inputs greater than -99mV, as - - -

***PATENT APPLIED FOR**

Reliability is assured by a low component count (14), low internal heat rise (10°C), and extensive factory testing and quality control procedures, including 168 hours of failure free burn-in. MTBF is 260,000 hours at +25°C.

PACKAGE AND INTERCONNECT
The AD2026 uses a new case and lens which assemble without hardware. A series of fingers molded as part of the case capture the PCB and permit snap-in mounting of the DPM in the front panel cutout. The lens has intentionally been left devoid of markings to permit the user to individualize the DPM with his logo, measurement information, styling touches and other proprietary data.

Connection to the AD2026 is made via Pins 1 through 5 and A through E. Pins 6, 7, F and H are not normally used (see Pin Connection Table). A suitable connector is the T & B/Ansley 609-1001M or the Berg, 3M or Spectra Strip equivalents. This type of connector allows fast crimp connection to ribbon cable. The Berg 47745 connector or the Amp equivalent offers convenient crimping to individual insulated wires.

DESIGNED AND BUILT FOR QUALITY AND RELIABILITY
The AD2026 uses the proven dual slope integrating A/D conversion technique. All analog and digital circuitry with the exception of the integrating capacitor and the components associated with decoding and driving the LED display are integrated on a single proprietary I^2L LSI chip. As a result, the total DPM consists of 14 electrical components and the normally conflicting objectives of low cost and high reliability are both achieved. Further, the manufacturing process is designed for achieving the economies of high volume, while at the same time, extensive testing, both in process and following final assembly, assures that the reliability potential of the product is achieved in practice.

Route 1 Industrial Park; P O. Box 280; Norwood, Mass. 02062
Tel: 617/329 4700 TWX: 710/394-6577
West Coast 213/595-1783 | Mid-West 312 894-3300 | Texas 214/231-5094

SPECIFICATIONS (typical at +25°C and nominal supply voltage unless otherwise noted)

DISPLAY OUTPUT
- Light emitting diode, planar seven segment display readouts, 0.5" (13mm) high for three data digits
- Overload Indication: EEE
- Negative Indication: -XX
- Negative Overload Indication: ---
- Decimal Points: three (3) selectable at input connector

ANALOG INPUT
- Configuration: Limited bipolar, balanced differential input
- Full Scale Range: -99mV to +999mV
- Automatic Polarity
- Input Impedance: 100MΩ
- Bias Current: 110nA
- Overvoltage Protection: ±15VDC, sustained

ACCURACY
- ±0.1% ±1 digit[1]
- Resolution: 1mV
- Temperature Range[2]: -10°C to +60°C operating; -25°C to +80°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: 10μV/°C (essentially auto zero)
- Warm-Up Time to Rated Accuracy: Instantaneous
- Settling Time to Rated Accuracy: 0.3 second for full input voltage swing

COMMON MODE REJECTION (1kΩ source imbalance, DC to 1kHz)
- 50dB

COMMON MODE VOLTAGE
- ±200mV

CONVERSION RATE
- 4 conversions per second
- Hold and read on command

CONTROL INPUTS

Display Blanking/Display Power Input: The display of the AD2026 can be blanked by removal of power to the display power input, with no effect on conversion circuitry. If external logic switching is used, the display requires 110mA peak (85mA average) when illuminated.

Hold: When the Hold input is at Logic "0", grounded or open circuit, the AD2026 will convert at 4 conversions per second. If a voltage of 0.6 to 2.4V is applied to this input, the DPM will stop converting and hold the last reading. A 12kΩ resistor in series with this input to +5V will provide the proper voltage input.

DECIMAL POINT
- To illuminate decimal points, ground appropriate pin (A, B or J)

POWER INPUT[3]
- Converter: +5V ±5%, 0.2 watts typ; 0.33 watts max
- Display: +5V ±40%, 0.45 watts typ, 0.75 watts max

CALIBRATION ADJUSTMENTS
- Gain
- Zero
- Recommended recalibration interval: six months

SIZE
- 3.43"W x 2.0"H x 0.85"D (87 x 52 x 22mm)
- 0.88" (22mm) overall depth to rear of connector
- Panel cutout required: 3.175 ±0.015" x 1.810 ±0.015" (80.65 ±0.38 x 45.97 ±0.38mm)

WEIGHT
- 1.8 ounces (53 grams)

CONNECTOR

A 10 pin T & B/Ansley 609-1001M with two feet of 10 conductor ribbon cable is available. Order AC2618 at $3.00 each.

NOTE: Conductor to pin A is color coded dark blue. Sequence of ribbon connections is A, 1, B, 2, C, 3, etc.

PRICING

$49 (1–9), $34 (100s), $29 (1000+)
Substantial OEM discounts available

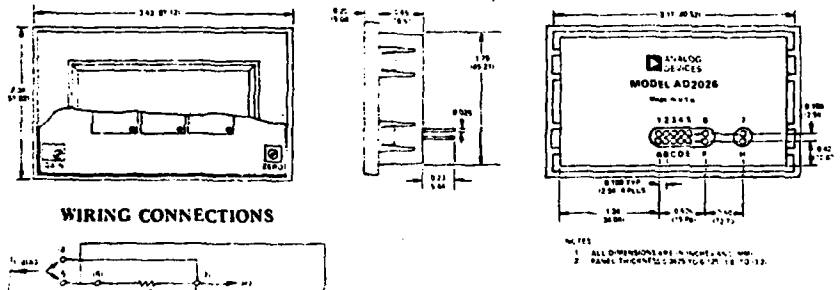
[1] Guaranteed at +25°C and nominal supply voltage
[2] Guaranteed
[3] When the same power supply is used to power both display and converter, +5V, ±5%, 0.65 watts typical, 0.9 watts max is required.

Specifications subject to change without notice.

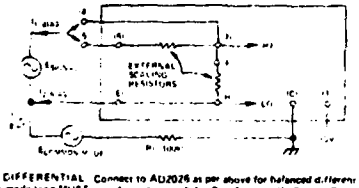
C3890—8—7/77

OUTLINE DIMENSIONS AND PIN CONNECTIONS

Dimensions shown in inches and (mm).



WIRING CONNECTIONS



BALANCED DIFFERENTIAL: Connect to AD2026 as per above for balanced differential input as shown. The common mode loop MUST provide a return path for Bias Currents (I_B, I_{B2}). Bias current of the AD2026. The resistance (R) of this path must be less than 100kΩ. CAUTION: Total Common Mode voltage between Pins E and C must not exceed 200mV.

EXTERNAL SCALING RESISTORS can be connected between Pins 6 and 7 and between Pins 7 and E. Use 9 or 5 at the High Analog Input when scaling resistors are used, and Pin 4 when they are not. Pin E is the Low Input in either case.

SINGLE ENDED INPUT: For single ended input, connect Pin C to Pin E.

PIN	FUNCTION
1	+5V Power
2	+5V Display Power
3	Decimal Point X.XX
4	Input Ribbon Scaling Resistors Not Used
5*	Input Ribbon Scaling Resistors Are Used
6*	Series Arm of Scaling Resistor Divider
7*	Series Arm of Scaling Resistor Divider

PIN	FUNCTION
A	Decimal Point X.X.X
B	Decimal Point XX.X
C	Power Ground
D	Hold
E	Analog Ground
F*	Shunt Arm of Scaling Resistor Divider
H*	Shunt Arm of Scaling Resistor Divider

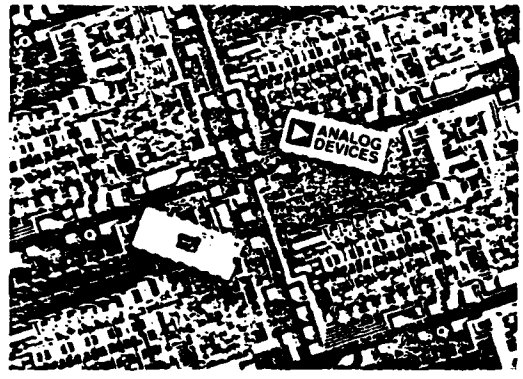
*NOT NORMALLY USED. ALLOWS CONVENIENT MOUNTING OF SCALING RESISTORS

PRINTED IN U.S.A.

ANALOG DEVICES

Low Cost 10-Bit Monolithic D/A Converter

PRELIMINARY TECHNICAL DATA



FEATURES

- Low Cost ($9.95 in 100's, AD561J)
- Complete Current Output Converter
- High Stability Buried Zener Reference
- Laser Trimmed to High Accuracy (1/4LSB Max Error, AD561K, T)
- Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges
- Fast Settling – 250ns to 1/2LSB
- Guaranteed Monotonicity Over Full Operating Temperature Range
- TTL/DTL and CMOS Compatible (Positive True Logic)
- Single Chip Monolithic Construction
- Hermetically-Sealed Ceramic DIP (All Grades)

PRODUCT DESCRIPTION

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of ±1/4LSB max for the K and T versions, and 1/2LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15ppm/°C; the T.C. is tested and guaranteed to 30ppm/°C max for the K and T versions, 60ppm/°C max for the S, and 80ppm/°C for the J.

All grades are packaged in a 16-pin hermetically-sealed ceramic dual-in-line package. The AD561J and K versions are specified for operation over the 0 to +70°C temperature range, the AD561S and T for operation over the full military temperature range from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4LSB max relative accuracy and 1/2LSB max differential nonlinearity. The low T.C. R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting V_{CC} to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25μA.
3. The high speed current steering switches are designed to settle in less than 250ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 to 5μs range.
4. The AD561 has an output voltage compliance range from -2 to +10 volts, thus allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40MΩ open collector output impedance results in negligible errors due to output leakage currents.
5. Every AD561 is subjected to long term stabilization bakes and temperature cycled ten times from -65°C to +150°C prior to final test to insure reliability and long-term stability.

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783 Mid-West 312/894-3300 Texas 214/231-5094

SPECIFICATIONS (T_A = +25°C, V_{CC} = +5V, V_{ee} = -15V, unless otherwise specified)

MODEL	AD561J MIN	AD561J TYP	AD561J MAX	AD561K MIN	AD561K TYP	AD561K MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			•			V
Bit OFF Logic "0"			+0.8			•	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			•			V
Bit OFF Logic "0"			30% V_{CC}			•	V
Logic Current (Each Bit)(T_{MIN} to T_{MAX})							
Bit ON Logic "1"		+5	+100		•	•	nA
Bit OFF Logic "0"		-5	-25		•	•	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	•	•	•	mA
Bipolar	±0.75	±1.0	±1.2	•	•	•	mA
Resistance (Exclusive of Application Resistors)		40M			•		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		•	•	% of F.S.
Capacitance		25			•		pF
Compliance Voltage	-2	-3	+10	•	•	•	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			•		ns
POWER REQUIREMENTS							
V_{CC}, +4.5VDC to +16.5VDC		8	10		•	•	mA
V_{EE}, -10.8 to -16.5VDC		12	16		•	•	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5VDC to +16.5VDC		2	10		•	•	ppm of F.S./%
V_{EE}, -10.8VDC to -16.5VDC		4	25		•	•	ppm of F.S./%
TEMPERATURE RANGE							
Operating		0 to +70			•	•	°C
Storage		-65 to +150			•	•	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	80		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT		0 to +10			•		V
RANGES (See Figs. 5, 6)		-5 to +5			•		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			•		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			•		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			•		% of F.S.
Bipolar Zero (With 20Ω Trimmer)		±0.2			•		% of F.S.

*Specifications same as AD561J specs.
Specifications subject to change without notice.

MODEL	AD561S MIN	AD561S TYP	AD561S MAX	AD561T MIN	AD561T TYP	AD561T MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			**			V
Bit OFF Logic "0"			+0.8			**	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			**			V
Bit OFF Logic "0"			30% V_{CC}			**	V
Logic Current (Each Bit)(T_{MIN} to T_{MAX})							
Bit ON Logic "1"		+20	+100		**	**	nA
Bit OFF Logic "0"		-25	-100		**	**	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	**	**	**	mA
Bipolar	±0.75	±1.0	±1.2	**	**	**	mA
Resistance (Exclusive of Application Resistors)		40M			**		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		**	**	% of F.S.
Capacitance		25			**		pF
Compliance Voltage	-2	-3	+10	**	**	**	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			**		ns
POWER REQUIREMENTS							
V_{CC}, +4.5VDC to +16.5VDC		8	10		**	**	mA
V_{EE}, -10.8 to -16.5VDC		12	16		**	**	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5VDC to +16.5VDC		2	10		**	**	ppm of F.S./%
V_{EE}, -10.8VDC to -16.5VDC		4	25		**	**	ppm of F.S./%
TEMPERATURE RANGE							
Operating		-55 to +125			**	**	°C
Storage		-65 to +150			**	**	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	60		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT		0 to +10			**		V
RANGES (See Figs. 5, 6)		-5 to +5			**		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			**		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			**		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			**		% of F.S.
Bipolar Zero (With 20Ω Trimmer)		±0.2			**		% of F.S.

**Specifications same as AD561S specs.
Specifications subject to change without notice.

DIGITAL LOGIC INTERFACE

All standard positive supply logic families interface easily with the AD561. The digital code is positive true binary (all bits high, logic "1", gives positive full scale output). The logic input load factor (100nA max at logic "1", -25μA max at logic "0", 3pF capacitance), is less than one equivalent digital load for all logic families, including unbuffered CMOS. The digital threshold is set internally as a function of the positive supply, as shown in Figure 1. For most applications, connecting V_{CC} to the positive logic supply will set the threshold at the proper level for maximum noise immunity. For nonstandard applications, refer to Figure 1 for threshold levels. Uncommitted bit input lines will assume a "1" state (similar to TTL), but they are high impedance and subject to noise pickup. Unused digital inputs should be connected directly to ground or V_{CC}, as desired.

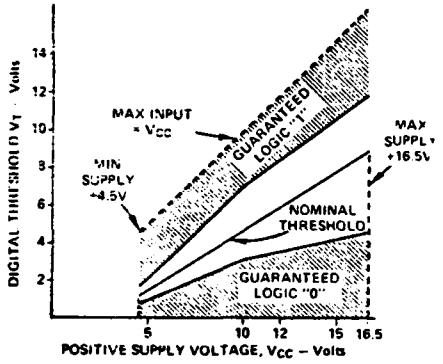
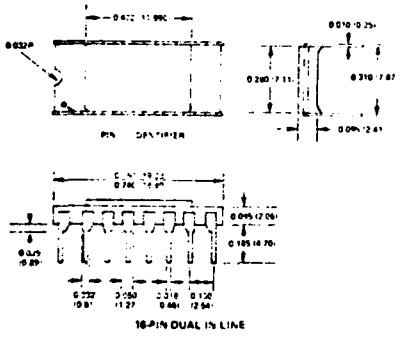


Figure 1. Digital Threshold Vs. Positive Supply



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Figure 2.

THE AD561 OFFERS TRUE 10-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see page 5) from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD561 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T versions − 1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD561 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 9.8mV change in the analog output (1LSB = 10V x 1/1024 = 9.8mV). If in actual use, however, a 1LSB change in the input code results in a change of only 2.45mV (1/4LSB) in analog output, the differential nonlinearity error would be 7.35mV, or 3/4LSB. The AD561K and T have a max differential linearity error of 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 2.5ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.025% (100 x 2.5ppm/°C of error). The resulting error could then be as much as 0.025% + 0.025% = 0.05% of F.S. (1/2LSB represents 0.05% of F.S.). To be sure of accurate performance all versions of the AD561 are therefore 100% tested to be monotonic over the full operating temperature range.

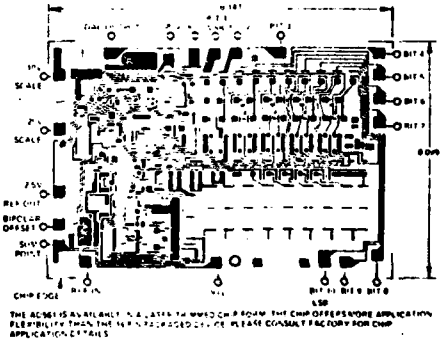


Figure 3. Chip Bonding Diagram

AD561 ORDERING GUIDE

MODEL	TEMP RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PRICE 1–24	25–99	100–999
AD561J	0 to +70°C	±1LSB max	80ppm max	$15.00	$12.50	$ 9.95
AD561K	0 to +70°C	±½LSB max	30ppm max	$22.50	$18.00	$15.00
AD561S	-55 to +125°C	±1LSB max	60ppm max	$27.00	$22.00	$18.00
AD561S/883B*	-55 to +125°C	±1LSB max	60ppm max	$35.00	$26.00	$24.00
AD561T	-55 to +125°C	±½LSB max	30ppm max	$48.00	$40.00	$32.00
AD561T/883B*	-55 to +125°C	±½LSB max	30ppm max	$60.00	$50.00	$40.00

*The AD561S/883B and AD561T/883B are fully processed to MIL-STD-883A, Method 5004, Class B.
The complete price list is available on request.

CONNECTING THE AD561 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming. (A 5mV op amp offset is equivalent to 1/2LSB on a 10 volt scale). If a 25Ω fixed resistor is substituted for the 50Ω trimmer, unipolar zero will typically be within ±1/10LSB (plus op amp offset), and full scale accuracy will be within ±1LSB. Substituting a 10Ω resistor for the 20Ω bipolar offset trimmer will give a bipolar zero error typically within ±1LSB.

The AD509 is recommended for buffered voltage-output applications which require a *settling time to ±½LSB of one* microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25picofarad DAC output capacitance.

FIGURE 5. UNIPOLAR CONFIGURATION
This configuration will provide a unipolar 0 to +10 volt output range.

STEP I . . . ZERO ADJUST
Turn all bits OFF and adjust op amp trimmer, R_1, until the output reads 0.000 volts (1LSB = 9.76mV).

STEP II . . . GAIN ADJUST
Turn all bits ON and adjust 50Ω gain trimmer, R_2, until the output is 9.990 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.23V full scale is desired (exactly 10mV/bit), insert a 120Ω resistor in series with R_2.

FIGURE 6. BIPOLAR CONFIGURATION
This configuration will provide a bipolar output voltage from -5.000 to +4.990 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . ZERO ADJUST
Turn ON MSB only, turn OFF all other bits. Adjust 20Ω trimmer R_3, to give 0.000 output volts.

STEP II . . . GAIN ADJUST
Turn OFF all bits, adjust 50Ω gain trimmer to give a reading of -5.000 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 7. ±10 VOLT BUFFERED BIPOLAR OUTPUT
The AD561 can also be connected for a ±10 volt bipolar range with an additional external resistor as shown in Figure 7. A larger value trimmer is required to compensate for tolerance in the thin film resistors (which are trimmed to match the full scale current). For best full scale temperature coefficient performance, the external resistors should have a T.C. of -50ppm/°C. For applications requiring optimum performance, a ±10 volt bonding option is available on special order.

PIN CONFIGURATION
TOP VIEW

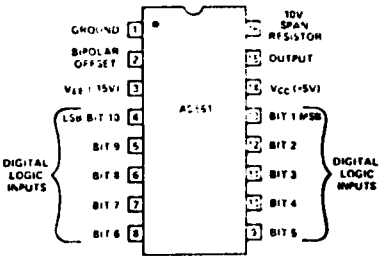


Figure 4.

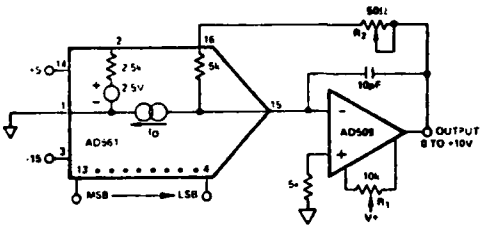


Figure 5. 0 to +10V Unipolar Voltage Output

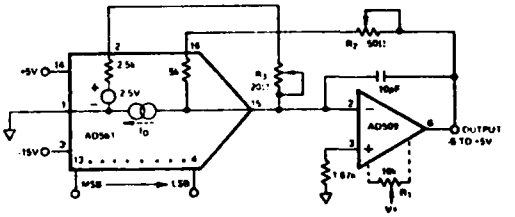


Figure 6. ±5V Buffered Bipolar Voltage Output

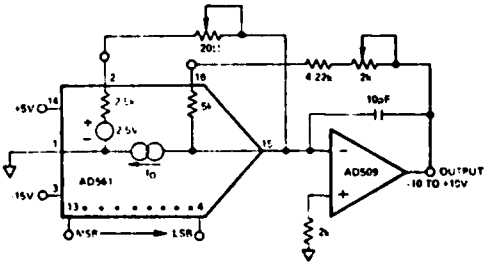


Figure 7. ±10V Buffered Voltage Output

CIRCUIT DESCRIPTION

A simplified schematic with the essential circuit features of the AD561 is shown in Figure 8. The voltage reference, CR1, is a buried zener (or subsurface breakdown device). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long term stability and lower noise are the major benefits the buried zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so that the positive supply can be allowed to go as low as 4.5 volts. The temperature coefficient of each diode is determined individually; this data is then used to laser trim a compensating circuit to balance the overall T.C. to zero. The typical resulting T.C. is 0 to ±15ppm/°C.

The negative reference level is inverted and scaled by A_1 to give a +2.5 volt reference (which can be driven by the low positive supply). The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the 2.5kΩ bipolar offset resistor; it can still be used as a voltage reference as shown below in Figure 9.

The 2.5kΩ scaling resistor and control amplifier A_2 then force a 1mA reference current to flow through reference transistor Q1, which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since Q_1 and Q_2 have equal emitter areas and have equal 5kΩ emitter resistors, Q_2 also carries 1mA. The ladder voltage drop constrains Q_7 (with area 4A) to carry only 0.5mA; Q_8 carries 0.25mA, etc.

The first four significant bit cells are scaled exactly in emitter area to match Q_1 for optimum V_{BE} and V_{BE} drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18mV V_{BE} difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is done by forcing 120μA through the 150Ω interbase resistors. These resistors and the R-2R ladder resistors are actively laser-trimmed at the wafer level to bring total device accuracy to better than ½LSB. Sufficient ratio accuracy in the last two bits is obtained by simple emitter area ratio such that it is unnecessary to use additional area for ladder resistors. The current in Q_{16} is added to the ladder to balance it properly but is not switched to the output; thus full scale is 1023/1024 x 2mA.

The switching cell of Q_3, Q_4, Q_5 and Q_6 serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, thus minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface) is applied to one side of each cell.

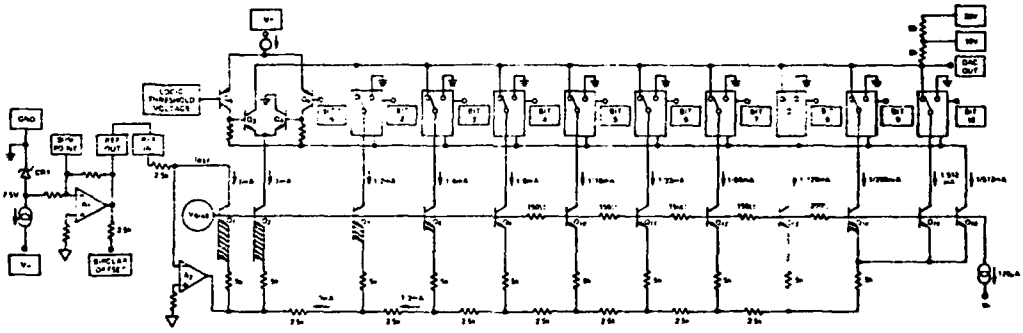


Figure 8. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

PRECISION LOW-NOISE REFERENCE

The precision reference of the AD561 can be brought out separately from the DAC to serve as a master system reference. Since the reference is connected through the 2.5kΩ bipolar offset resistor, it must be buffered externally, as shown here in Figure 9. The DAC section can still be operated independently in a unipolar mode, but internal thermal and ground loop effects will create crosstalk of about 0.01% with an ideal ground. The long term stability of this reference will be especially good, typically ±0.01% per year or better. If the filter capacitor, C is not used, wideband output noise will be about 120ppm p-p (1.2mV p-p for 10 volts). If C is 4.7μF, wideband noise will be about 25μV p-p (10 volts out) and 15μV p-p from 0.1 to 10Hz.

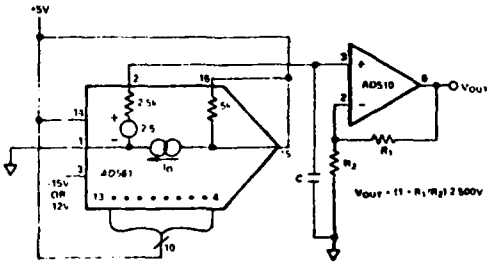


Figure 9. Precision Ultra Low Noise Reference

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD561 are specifically designed for fast settling operation. The typical settling time to ±0.05% (½LSB) for the worst case transition (major carry, 0111111111 to 1000000000) is less than 250ns, the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB.) But full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing

The settling time for the AD561 is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see page 8), or in many display applications. This form of conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 12. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD561 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.05% of full scale (for a full scale transition) requires 7.6 time constants. This effect is important for $R > 1k\Omega$

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits on page 5 using the fast settling AD509. The circuits shown settle to ±½LSB in 600ns unipolar and 1.1μs bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices; 0.1μF will be sufficient since the AD561 runs at constant supply current regardless of input code.

POWER SUPPLY SELECTION

The AD561 will operate over a wide range of power supply voltages, with a total supply from 15.3 to 33 volts. Symmetrical supplies are not required, and in many applications not recommended. Maximum allowable supplies are ±16.5V.

The positive supply level determines the digital threshold level, as explained on page 4 and shown in Figure 1. It is therefore recommended that V_{CC} be connected directly to the digital supply for best threshold match.

Positive output voltage compliance range is unaffected by the positive supply level because of the open collector output stage design, thus the full +10 volt compliance is available even with a +5 volt V_{CC} level. Power supply rejection is excellent, so that digital supply noise will not be reflected to the output but use of a 0.1μF bypass capacitor near the AD561 is recommended for decoupling.

The nominal negative supply level is -15 volts, with an allowable range of -10.8 to -16.5 volts. The negative supply level affects the negative compliance range, as shown in Figure 10

OUTPUT VOLTAGE COMPLIANCE

The AD561 has a typical output compliance range from -3 to +10 volts. The output current is unaffected by changes in the output terminal voltage over that range. This results from the use of open collector output switching stages in a cascode configuration, and gives an output impedance of 40MΩ. Positive compliance range is limited only by collector breakdown (and is independent of positive supply level), but the negative range is limited by the required bias levels and resistor ladder voltage. Negative compliance varies with negative supply, as shown in Figure 10. The compliance range is guaranteed to be -2 to +10 volts with V_{EE} = -15 volts.

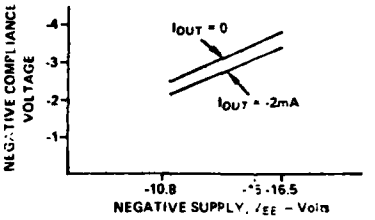


Figure 10 Typical Negative Compliance Range Vs. Negative Supply.

DIRECT UNBUFFERED VOLTAGE OUTPUT

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 1 shows a connection using the gain and bipolar output resistors to give a ±1.66 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 2.5 volt reference voltage for bipolar offset. For example, setting R_X = 2.5kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance. A 0 to +10 volt output can be obtained by connecting the 5kΩ gain resistor to 9.99 volts; again the digital code is complementary binary.

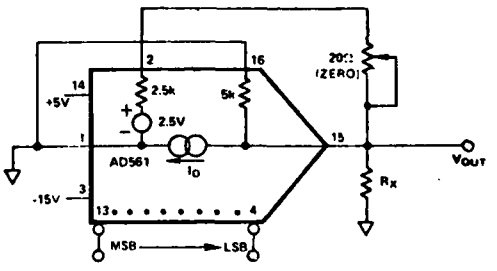


Figure 11 Unbuffered Bipolar Voltage Output

HIGH SPEED 10-BIT A/D CONVERTERS

The fast settling characteristics of the AD561 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 10-bit converter system to be constructed with a minimum parts count. Shown here is a configuration using standard components; this system completes a full 10-bit conversion in 5.5μs unipolar or 12μs bipolar. This converter will be accurate to ±1/2LSB of 10 bits and have a typical gain T.C. of 10ppm/°C.

In the unipolar mode, the system range is 0 to 9.99 volts, with each bit having a value of 9.76mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +4.9mV (trim R_1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9935 volts (10 volts − 1LSB + 1/2LSB); then trim R_2 again until the LSB just begins to appear (all other bits "1").

The bipolar signal range is -5.0 to +4.99 volts. Bipolar offset trimming is done by applying a +4.9mV input signal and trimming R_1 for the LSB transition (MSB "1", all other bits "0"). Full scale is set by applying +4.995 volts and trimming R_2 for the LSB transition (all other bits "0"). In many applications, the prettrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 10 bit ±½LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance of 1kΩ, 1LSB = 2mV) to the point that comparator performance will be sacrificed. A 1kΩ resistor is the optimum value for this application for 10-bit accuracy. The chart shown in the figure gives the speed of the ADC for ±1/2LSB accuracy (and no missing codes) for 6, 8 and 10-bit resolution.

A much faster converter can be constructed by using higher performance external components. Each individual high-order bit settles in less than 250ns, the low-order bits less than 200ns. Because of this, a staged clock which speeds up for lower bits will improve the speed. Also, a faster comparator and Schottky TTL or ECL logic would be necessary. 10-bit converters in the 3 to 5μs range could be built around the AD561 with these techniques.

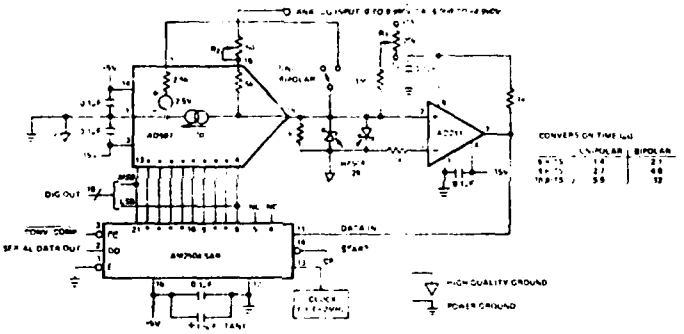


Figure 12. Fast Precision Analog to Digital Converter

DIGITAL 4 TO 20mA OR 1 TO 5 VOLT CONVERTER

A direct digital 4 to 20mA or 1 to 5 volt line driver can be built with the AD561 as shown in Figure 13. The 2.5 volt reference is divided to provide 1 volt at the op amp noninverting input — thus a zero input code results in a 1 volt output at the Darlington emitter (V_{OUT}). The 2k feedback resistance converts the nominal 2mA (±20%) full scale output from the AD561 to 4 volts, for a total output of 5 volts F.S. The voltage at the emitter forces a proportional current through the 250Ω (which appears at the collector as I_{OUT}). The AD561 current is added to the 4−20mA line; thus 5 volts full scale gives 22mA in the current loop. For exactly 20mA, trim the 1k pot for 4.5V F.S. (A single op amp circuit will not produce both 1 to 5 volt and 4 to 20mA outputs simultaneously.)

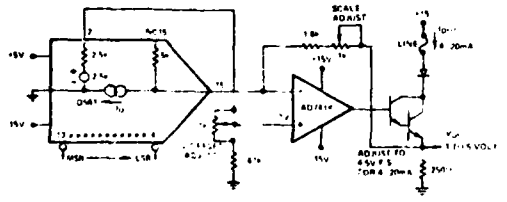


Figure 13. Digital 4 to 20mA or 1 to 5 Volt Line Driver

DIGITALLY PROGRAMMABLE SETPOINT COMPARATOR

Figure 14 demonstrates a high accuracy systems-oriented setpoint comparator. The 2.5 volt reference is buffered and amplified by the AD741K to produce an exact 10.000 volt reference which could be used as a primary system reference for several such circuits. The +10 volt compliance of the AD561 then allows it to generate a zero to +10 volt output swing through the 5kΩ application resistor without an additional op amp. The digital code for this system will be complementary binary (all 1's give 0.00 volts out).

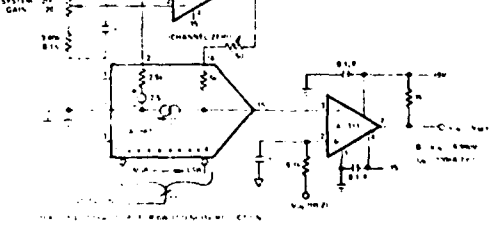


Figure 14. Digitally Programmable Set Point Comparator

Operational Amplifiers

LM108A/LM208A/LM308A operational amplifier

general description

The LM108A, LM208A and LM308A are precision operational amplifiers having specifications about a factor of ten better than FET amplifiers over their operating temperature range. In addition to low input currents, these devices have extremely low offset voltage, making it possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary. Outstanding characteristics include:

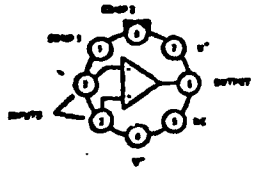
- Offset voltage guaranteed less than 0.5 mV
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed 5 μV/°C drift.

The low current error of the LM108A series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

The LM208A is identical to the LM108A, except that the LM208A has its performance guaranteed over a -25°C to 85°C temperature range, instead of -55°C to 125°C. The LM308A has slightly-relaxed specifications and has its performance guaranteed over a 0°C to 70°C temperature range.

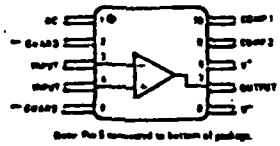
connection diagrams *

Metal Can



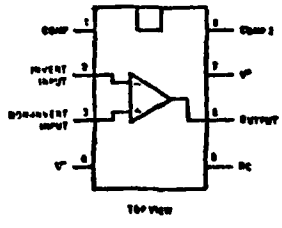
Order Number LM108AH or LM208AH or LM308AH
See Package 11

Flat Package



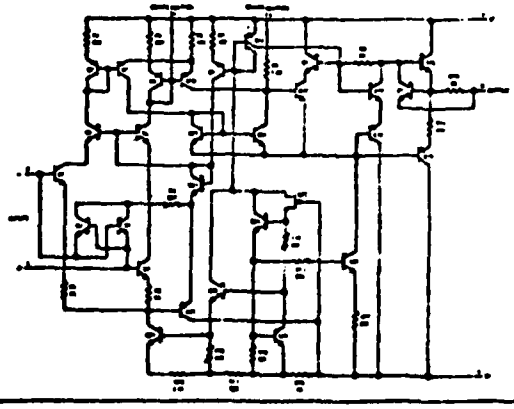
Order Number LM108AF or LM208AF or LM308AF
See Package 3

Dual-In-Line

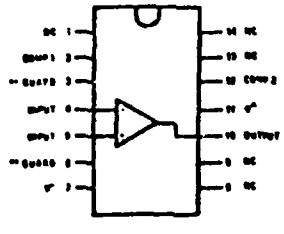


Order Number LM308AN
See Package 20

schematic diagram *



Dual-In-Line



Order Number LM108AD or LM208AD or LM308AD
See Package 1

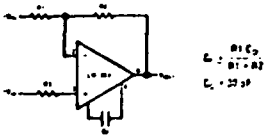
LM108A/LM208A

absolute maximum ratings

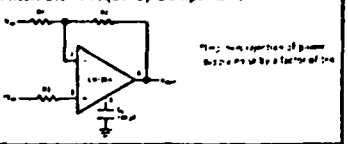
Supply Voltage		±20V
Power Dissipation (Note 1)		500 mW
Differential Input Current (Note 2)		±10 mA
Input Voltage (Note 3)		±15V
Output Short-Circuit Duration		Indefinite
Operating Temperature Range	LM108A	-55°C to 125°C
	LM208A	-25°C to 85°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

compensation circuits

Standard Compensation Circuit



Alternate* Frequency Compensation



electrical characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$		0.3	0.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0	nA
Input Resistance	$T_A = 25°C$	30	70		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 10$ kΩ	80	300		V/mV
Input Offset Voltage				1.0	mV
Average Temperature Coefficient of Input Offset Voltage			1.0	5.0	μV/°C
Input Offset Current				0.4	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5	pA/°C
Input Bias Current				3.0	nA
Supply Current	$T_A = +125°C$		0.15	0.4	mA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10$ kΩ	40			V/mV
Output Voltage Swing	$V_S = ±15V$, $R_L = 10$ kΩ	±13	±14		V
Input Voltage Range	$V_S = ±15V$	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB

Note 1: The maximum junction temperature of the LM108A is 150°C, while that of the LM208A is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $±5V \leq V_S \leq ±20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM208A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$.

LM308A

absolute maximum ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$		0.3	0.5	mV
Input Offset Current	$T_A = 25°C$		0.2	1	nA
Input Bias Current	$T_A = 25°C$		1.5	7	nA
Input Resistance	$T_A = 25°C$	10	40		MΩ
Supply Current	$T_A = 25°C$, $V_S = ±15V$		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 10 k\Omega$	80	300		V/mV
Input Offset Voltage				0.73	mV
Average Temperature Coefficient of Input Offset Voltage			1.0	5.0	μV/°C
Input Offset Current				1.5	nA
Average Temperature Coefficient of Input Offset Current			2.0	10	pA/°C
Input Bias Current				10	nA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10 k\Omega$	60			V/mV
Output Voltage Swing	$V_S = ±15V$, $R_L = 10 k\Omega$	±13	±14		V
Input Voltage Range	$V_S = ±15V$	±14			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB

Note 1: The maximum junction temperature of the LM308A is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $±5V \leq V_S \leq ±15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified.

Operational Amplifiers

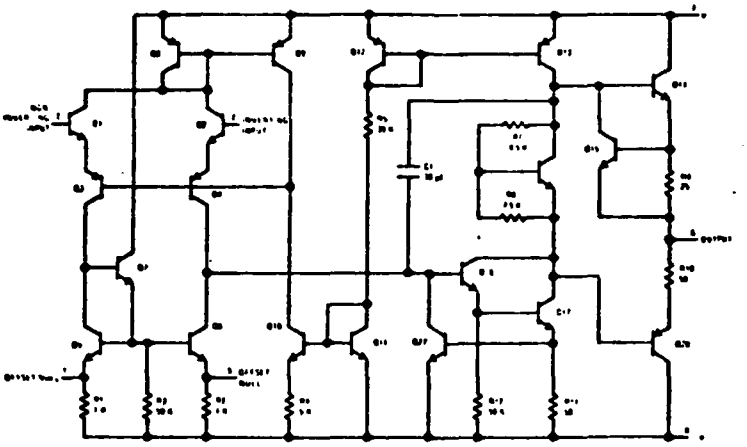
LM741/LM741C operational amplifier general description

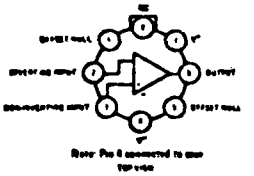
The LM741 and LM741C are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The offset voltage and offset current are guaranteed over the entire common mode range. The amplifiers also offer many features which make their application nearly foolproof: overload protection on the input and output, no latch up when the common mode range is exceeded, as well as freedom from oscillations.

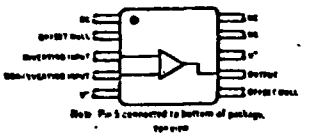
The LM741C is identical to the LM741 except that the LM741C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to 125°C.

schematic and connection diagrams

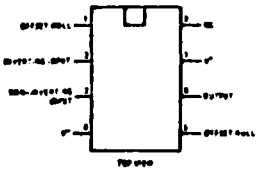




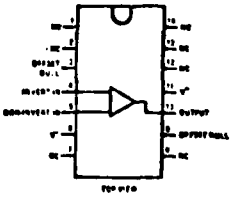
Order Number LM741H or LM741CH
See Package 11



Order Number LM741F
See Package 3



Order Number LM741CN
See Package 20



Order Number LM741CD
See Package 1
Order Number LM741CN-14
See Package 22

absolute maximum ratings

Supply Voltage	LM741	±22V
	LM741C	±18V
Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short Circuit Duration		Indefinite
Operating Temperature Range	LM741	−55°C to 125°C
	LM741C	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	LM741			LM741C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		30	200		30	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current	$T_A = 25°C$, $V_S = ±15V$		1.7	2.8		1.7	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 2k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S < 10k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 2k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = ±15V$, $R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = ±15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S < 10k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the LM741 is 150°C, while that of the LM741C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = ±15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM741C, however, all specifications are limited to $0°C \leq T_A \leq 70°C$ and $V_S = ±15V$.

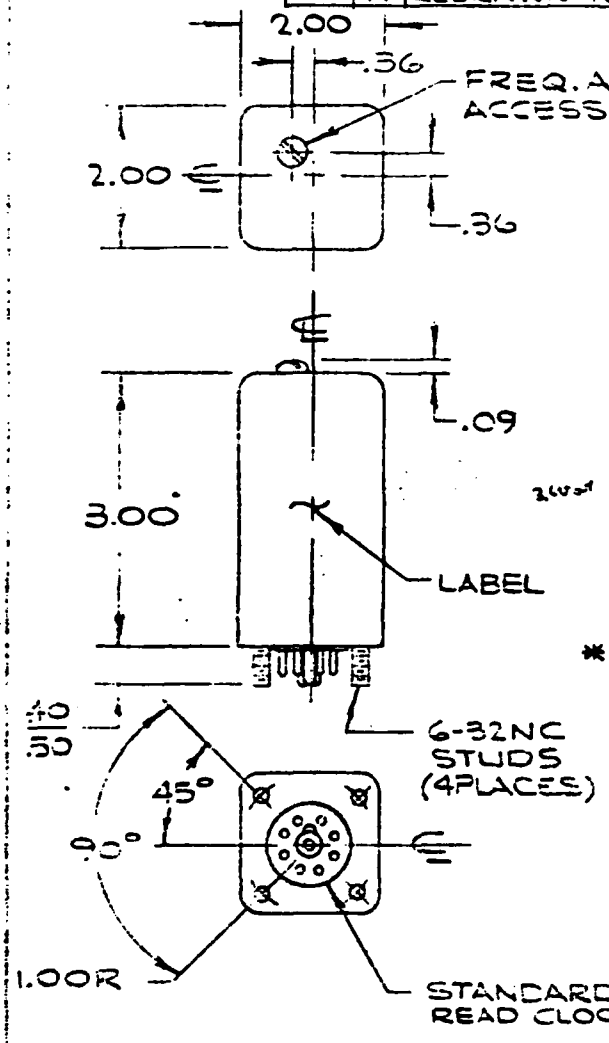
	Best long stability (highest output level)	Intermediate (long stability)	Most economical	5 VDC input for oven and oscillator
	CO-200 SERIES	**CO-211-1 SERIES**	**CO-211 SERIES**	**CO-211-5 SERIES**
Stability (Aging Rate)	*CO-205: 5 x 10 $^{-10}$/day CO 206: 1 x 10 $^{-9}$/day CO-203: 3 x 10 $^{-9}$/day CO-202: 5 x 10 $^{-9}$/day CO-201: 1 x 10 $^{-8}$/day	*CO 216-1: 5 x 10 $^{-10}$/day CO 217-1: 1 x 10 $^{-9}$/day CO 218-1: 3 x 10 $^{-9}$/day CO-215-1: 5 x 10 $^{-9}$/day CO-214-1: 1 x 10 $^{-8}$/day	CO 217: 1 x 10 $^{-9}$/day CO 218: 3 x 10 $^{-9}$/day CO 215: 5 x 10 $^{-9}$/day CO-214: 1 x 10 $^{-8}$/day CO-211: 1 x 10 $^{-7}$/day	*CO 216-5: 5 x 10 $^{-10}$/day CO 217-5: 1 x 10 $^{-9}$/day CO 218-5: 3 x 10 $^{-9}$/day CO 215-5: 5 x 10 $^{-9}$/day CO-214-5: 1 x 10 $^{-8}$/day

*(5 x 10 $^{-10}$/day average aging rate models are only available at 1, 2, 4 and 5 MHz with sine or logic out, or 10 MHz with sine output)

Output Frequency:	1 MHz, 2 MHz, 4 MHz, 5 MHz or 10 MHz standard (other frequencies available)			
Output Level:	>1 vrms into 50 ohms	>1 vrms into 500 ohms (TTL, ECL, CMOS compatible output or other sinewave levels optional)	>1 vrms into 500 ohms	TTL Compatible Drives 10 TTL loads
Frequency Offset vs:				
Supply ± 5%:	< ± 2 x 10 $^{-9}$	< ± 5 x 10 $^{-9}$	< ± 5 x 10 $^{-9}$	± 2 x 10 $^{-8}$
Load ± 10%:	< ± 1 x 10 $^{-9}$	< ± 5 x 10 $^{-9}$	< ± 1 x 10 $^{-8}$	
Temperature:				
0°C to + 50°C:	< ± 5 x 10 $^{-9}$	< ± 1 x 10 $^{-8}$	< ± 5 x 10 $^{-9}$	± 3 x 10 $^{-8}$
− 20°C to + 70°C:	< ± 1 x 10 $^{-8}$	< ± 3 x 10 $^{-8}$	Optional	Optional Option "A": ± 1 x 10 $^{-8}$ over 0°C to + 50°C Option "B": ± 3 x 10 $^{-8}$ over − 20°C to + 70°C
	(Higher stability and wider temperature range operation available)			
Short Term Stability:	< 1 x 10 $^{-10}$/sec	< ± 1 x 10 $^{-10}$/sec	< 1 x 10 $^{-10}$/sec	< 1 x 10 $^{-10}$/sec
Phase Noise (SSB dB/Hz)				
100 Hz from carrier:	− 115 dB	− 115 dB	− 115 dB	
1 KHz from carrier	− 135 dB	− 135 dB	− 135 dB	
	(Up to 15 dB improvement available, depending upon frequency)			
Input Voltage:	24 VDC standard	24 VDC standard	24 VDC standard	5 VDC
	(Operation from any specified voltage between 5 VDC and 32 VDC optional)			
Input Power: Turn on	6 watts	6 watts	6 watts	6 watts
Stabilized at 25°C.	3 watts	3 watts	3 watts	3 watts
	(Units with reduced power drain available)		(Units with reduced power drain available)	
Harmonics:	20 dB below desired output. If internal multiplication is used, subharmonics are also down 20 dB.			
(sinewave units)	*Harmonic and subharmonic attenuation can be improved on special order.*			
Frequency Adjustment:	Range sufficient to compensate for 5-10 years of crystal aging. Settable to < 1 x 10 $^{-8}$; use "V" option for improved settability			
Oven Control:	Proportional	Proportional	Proportional	Proportional
Size/Weight:	2" x 2" x 4", 10 oz. (51 x 51 x 102 mm, 0.3 Kgm)	2" x 2" x 3", 7 oz. (51 x 51 x 76 mm, 0.2 Kgm)	2" x 2" x 3", 7 oz. (51 x 51 x 76 mm, 0.2 Kgm)	2" x 2" x 3", 7 oz. (51 x 51 x 76 mm, 0.2 Kgm)
Base:	Standard: Octal plug and four studs Option H: 8 pin solder header in place of octal plug Option U: UG1819/U output connector, 7 pin solder header and 4 studs Option W: SMA output connector, 7 pin solder header and 4 studs Option X: BNC output connector, 7 pin solder header and 4 studs Other mechanical configurations available			
Option "V" (Electronic Tuning)	VCXO operation permits remote frequency adjustment or locking onto an external frequency source Add "V" to Model Number (e.g., CO-216V). Nominal range with 0-5V control is 3 x 10 $^{-7}$ (wider deviations available)			
Option "D" (Reduced Size)	Unit provides same performance as CO-211, CO-211-1 and CO-211-5 Series oscillators but in 1⅛" x 1⅛" x 3" package (volume reduction more than 40%).			

For higher stability models, see literature covering the CO-244V and CO-246V. For higher frequency models, see literature covering VHF oscillators

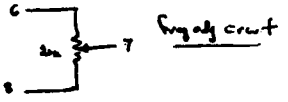
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REDRAWN TO NEW FORMAT	2-24-69	



TERM.	FUNCTION
1	R F OUTPUT
2	CASE
**3	D.C. INPUT (OV)
* 4	D.C. INPUT (+)
**5	RF RETURN
* 6	VCXO SUPPLY
* 7	VCXO INPUT
* 8	VCXO RETURN

*UNITS WITH VOLTAGE FREQ CONTROL ONLY.

**UNITS WITH SQUARE WAVE LOGIC LEVEL OUTPUT PINS 3 & 5 ARE INTERNALLY CONNECTED.



DO NOT SCALE DRAWING

DRAWING STARTED

S. Marino 2/24/69

VECTRON LABORATORIES, INC.

NORWALK, CONN.

INSTALLATION

CO211 SERIES OSC

SIZE	CODE IDENT NO	
A	27802	211-00-006A

SCALE 1/2 SHEET

DISTRIBUTION LIST

	No. of Copies
Office of Naval Research 800 N. Quincy Street Arlington, Virginia 22217 Attn: Code 222	2
102-CS	1
480	1
Director Naval Research Laboratory 4555 Overlook Avenue S.W. Washington, D.C. 20375	6
Director Office of Naval Research Branch Office 1030 East Green Street Pasadena, California 91106	1
Director Office of Naval Research Branch Office 495 Summer Street Boston, Massachusetts 02210	1
Director Office of Naval Research Branch Office 536 South Clark Street Chicago, Illinois 60605	1
Commander Naval Surface Weapons Center Acoustics Division White Oak Silver Springs, Maryland 20910 Attn: Dr. Zaka Slawsky	1
Commanding Office Office of Naval Research Branch Office Box 39 FPO New York 09510	1
Officer in Charge Naval Ship Research and Development Center Annapolis Laboratory Annapolis, Maryland 21402	1

DISTRIBUTION LIST

Commander
Naval Sea Systems Command, Nat. Center # 2
2521 Jefferson Davis Highway
Arlington, Virginia 20360
Attn: SEA 037 — 1
Carey Smith, 06HI — 1
David F. Bolka, 06H2 — 1

Commanding Office
Fleet Numerical Weather Control
Monterey, California 93940 — 1

Defense Documentation Center
Cameron Station
Alexandria, Virginia 22314 — 12

Director of Navy Laboratories
Chief of Naval Material
2211 Jefferson Davis Highway
Crystal Plaza #5
Arlington, Virginia 20360
Attn: Dr. James Probus, MAT 03L — 1

Commander
Naval Electronic Systems Command
2511 Jefferson Davis Highway, Nat. Center #1
Arlington, Virginia 20360
Attn: CDR A. R. Miller, ELEX 320 — 1

Commander Naval Ship Research & Development Center
Department of the Navy
Bethesda, Maryland 20084
Attn: Mr. Craig Olson — 1
Unclassified Library — 1

Chief of Naval Operations
Room 4D518, Pentagon
Washington, D.C. 20350
Attn: CAPT. A. H. Gilmore — 1

Commander
Naval Ocean Systems Center
Department of the Navy
San Diego, California 92132
Attn: Dr. Dan Andrews — 1
Mr. Henry Aurand — 1
Dr. Dean Hanna — 1

DISTRIBUTION LIST

Superintendent
Naval Research Laboratory
Underwater Sound Reference Division
P. O. Box 8337
Orlando, Florida 32806 — 1

Commanding Officer
Naval Underwater Systems Center
New London Laboratory
New London, Connecticut 06320
Attn: Dr. A. Nuttal — 1
Mr. A. Ellinthorpe — 1
Dr. D. M. Viccione — 1

Commander
Naval Air Development Center
Department of the Navy
Warminster, Pennsylvania 18974
Attn: Unclassified Library — 1

Commanding Office
Naval Coastal Systems Laboratory
Panama City, Florida 32401
Attn: Unclassified Library — 1

Superintendent
U.S. Naval Academy
Annapolis, Maryland, 21402
Attr: Library — 1

Superintendent
Naval Postgraduate School
Monterey, California 93940
Attn: Unclassified Library — 1

Commanding Officer
Naval Intelligence Support Center
4310 Suitland Road
Suitland, Maryland 20390
Attn: Dr. Johann Martinek — 1
Mr. E. Bissett — 1

Commanding Office
Naval Underwater Systems Center
Newport Laboratory
Newport, Rhode Island 02840
Attn: Unclassified Library — 1

DISTRIBUTION LIST

Applied Research Laboratories
University of Texas at Austin
P.O. Box 8029
10000 FM Road 1325
Austin, Texas 78712
Attn: Dr. Lloyd Hampton 1
Dr. Charles Wood 1

Commander
Naval Sea Systems Command
Washington, D.C. 20362
Attn: Unclassified Library, SEA 03E 1

Dr. Melvin J. Jacobson
Rensselaer Polytechnic Institute
Troy, New York 12181 1

Dr. T. G. Birdsall
Cooley Electronics Laboratory
The University of Michigan
Ann Arbor, Michigan 48109 1

Dr. Harry DeFerrari
The University of Miami
Rosenstiel School of Marine &
Atmospheric Sciences
4600 Rickenbacker Causeway
Miami, Florida 33149 1

Dr. M. A. Basin
S.D.P., Inc.
15250 Ventura Boulevard
Suite 518
Sherman Oaks, California 91403 1

Dr. Walter Duing
The University of Miami
Rosenstiel School of Marine &
Atmospheric Sciences
4600 Rickenbacker Causeway
Miami, Florida 33149 1

Dr. David Middleton
127 East 91st Street
New York, New York 10028 1

Dr. Donald W. Tufts
The University of Rhode Island
Kingston, Rhode Island 02881 1

DISTRIBUTION LIST

Dr. Loren W. Nolte
Duke University
Department of Electrical Engineering
Durham, North Carolina 27706 — 1

Mr. S. W. Autrey
Hughes Aircraft Company
P. O. Box 3310
Fullerton, California 92634 — 1

Dr. Thomas W. Ellis
Texas Instruments, Inc.
13500 North Central Expressway
Dallas, Texas 75231 — 1

Dr. Terry Ewart
Applied Physics Laboratory
The University of Washington
1013 Northeast Fortieth Street
Seattle, Washington 98195 — 1

Institute for Acoustical Research
Miami Division of the Palisades Geophysical Institute
615 S.W. 2nd Avenue
Miami, Florida 33130
Attn: Mr. M. Kronengold — 1
Dr. J. Clark — 1
Dr. S. Adams — 1

Mr. Carl Hartdegen
Palisades Geophysical Institute
Sofar Station
FPO New York 09560 — 1

Special Assistant for ASW
Office of the Assistant Secretary of the Navy for Research, Engineering & Systems
Washington, D.C. 20350
Attn: Dr. D. Hyde — 1

Mr. Beaumont Buck
Polar Research Laboratory
123 Santa Barbara Avenue
Santa Barbara, California 93101 — 1

Dr. M. Weinstein
Underwater Systems, Inc.
8121 Georgia Avenue
Silver Springs, Maryland 20910 — 1

DISTRIBUTION LIST

Mr. Thomas G. Kincaid
General Electric Company
P. O. Box 1088
Schenectady, New York 12301 — 1

Dr. E. G. Baxa, Jr.
Research Triangle Institute
Research Triangle Park
North Carolina 27709 — 1

Woods Hole Oceanographic Institution
Woods Hole, Massachusetts 02543
Attn: Dr. Paul McElroy
Dr. R. Spindel — 1

Mr. John Bouyoucos
Hydroacoustics, Inc.
321 Northland Avenue
P. O. Box 3813
Rochester, New York 14610 — 1

Maj R. J. Carpinella
Wright-Patterson AFB
Dayton, Ohio 45433 — 1

Atlantic Oceanographic & Meteorological
Laboratories
15 Rickenbacker Causeway
Miami, Florida 33149
Attn: Dr. John Proni — 1

Dr. C. N. K. Mooers
The University of Delaware
Newark, Delaware 19711 — 1

Dr. Stuart Schwartz
Princeton University
Department of Electrical Engineering
Brackett Hall, Engineering Quad.
Princeton, New Jersey 08540 — 1

Mr. Ray Veenkant
Texas Instruments, Inc.
North Central Expressway
MS 208
Dallas Texas 75222 — 1

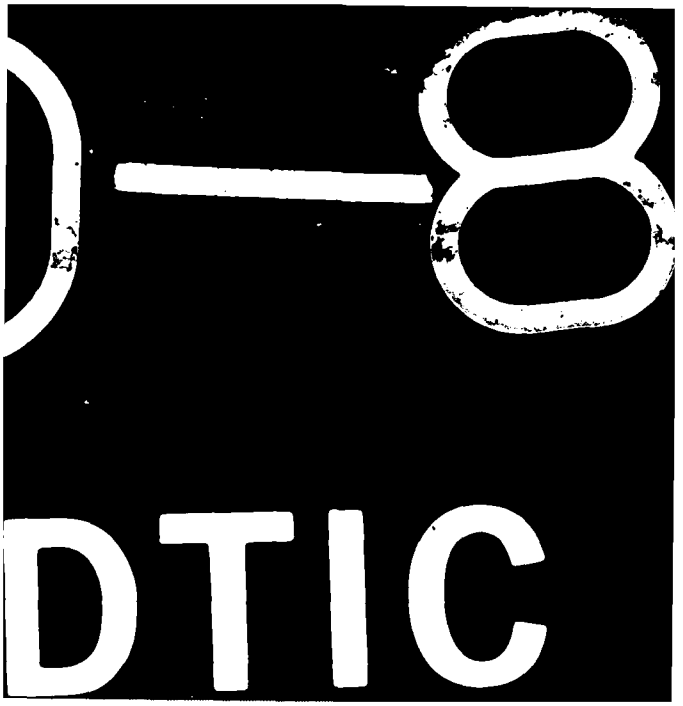
DISTRIBUTION LIST

Mr. William Graham
BDS/Technology
7908 Pine Road
Wyndmoor, Pennsylvania 19118 — 1

Dr. C. V. Kimball
Schlumberger
Schlumberger Doll Research Center
P. O. Box 307
Ridgefield, Connecticut 06877 — 1

Dr. Wm. Jobst
Code 3443
U.S. Naval Oceanographic Office
Bay St. Louis, Mississippi 39522 — 1

Cooley Electronics Laboratory
The University of Michigan
Ann Arbor, Michigan 48109 — 25


D-8
DTIC